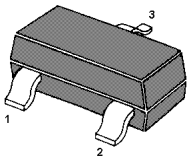
Features

- TrenchMOS™ technology
- Very fast switching
- Logic level compatible
- Subminiature surface mount package.

Package



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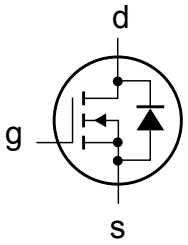
Marking

- Marking: N20



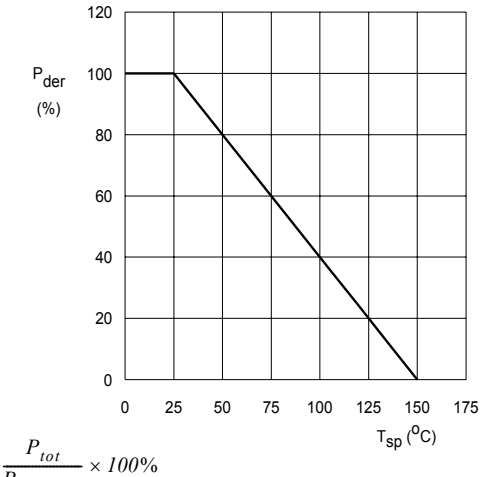
Absolute Maximum Ratings Ta = 25℃

Parameter		Symbol	Rating	Unit
Drain-source voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	Ta = 25℃	I_D	173	mA
	Ta = 100 ℃		110	
Pulsed Drain Current		I_{DM}	700	
Power dissipation	T_A = 25℃	P_D	0.83	W
Maximum Junction-to-Ambient		R_{thJA}	350	K/W
Thermal resistance from junction to solder point		R_{thJP}	150	
Operating and storage junction temperature range		T_J, T_{stg}	- 65+150	℃

Electrical Characteristics Ta = 25 ℃

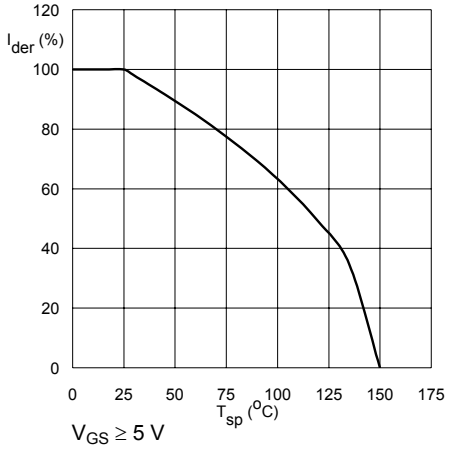
Parameter	Symbol	Test conditons	Min	Typ	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V , I_D=10 μA	50			V
Gate-threshold voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D= 1 mA	0.4	1.5	2	
Gate-body leakage	I_{GSS}	V_{DS} =0V , V_{GS} = ±20 V			±100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} =40 V , V_{GS} =0 V			1	uA
		V_{DS} =40 V , V_{GS} =0 V , Ta = 150℃			10	
Drain-source on-resistance	$R_{DS(0n)}$	V_{GS}= 10 V, I_D= 100 mA		2.8	15	Ω
		V_{GS}=5 V , I_D=100 mA		3.8	20	
Forward tran conductance	g_{fs}	V_{DS} =10 V , I_D= 100 mA	40	170		ms
Input capacitance	C_{iss}	V_{DS} =10 V , V_{GS} =0 V , f=1 MHz		17	25	pF
Output capacitance	C_{OSS}			7	15	
Reverse transfer capacitance	C_{rSS}			4	8	
Turn-on Time	$t_{d(0n)}$	V_{DD}=20V,R_D=180Ω		1.7	8	ns
Turn-off Time	$t_{d(off)}$	R_{GS}=50Ω,V_{GS} =10V R_G=50Ω		8	15	
Reverse recovery time	t_{rr}	I_S= 180mA;dI/dt=100A/μs;V_{GS} =0V;		30		
Recovered charge	Q_{rr}	V_{DS} =25V		30		nC
Diode forward voltage	V_{SD}	I_S= 180mA V_{GS}=0 V		0.9	1.5	V

Typical Characteristics



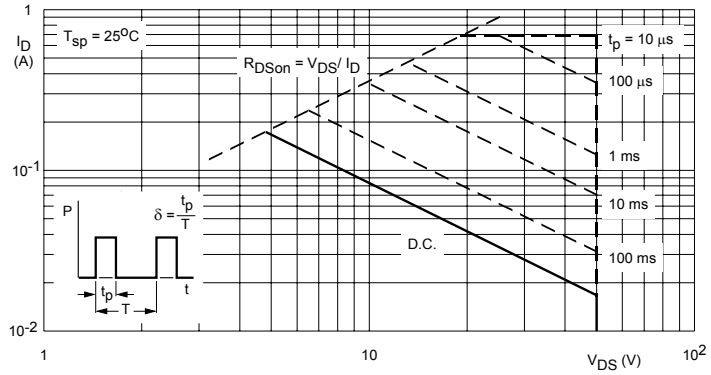
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature.



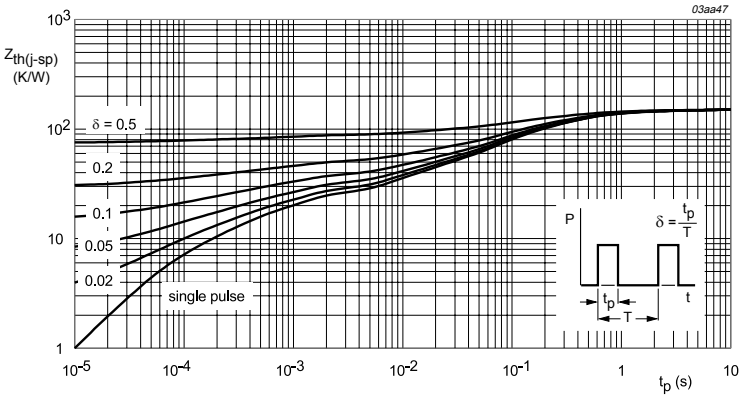
$$I_{der} = \frac{I^{D}}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



T_{sp} = 25 °C; I_{DM} is single pulse.

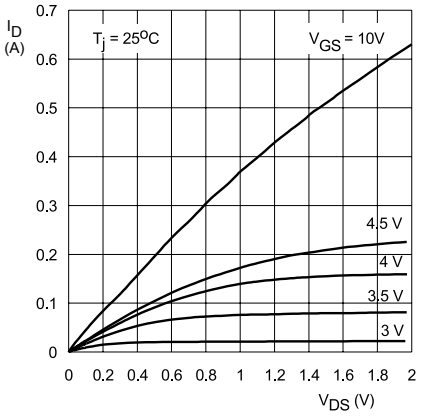
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.



Mounted on a metal clad substrate.

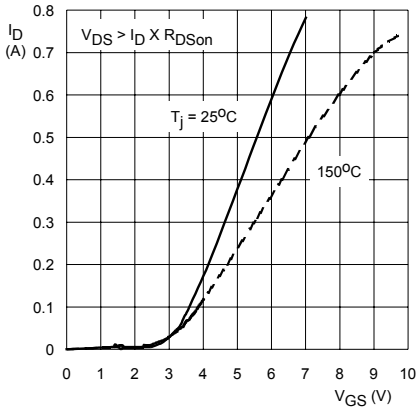
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

Typical Characteristics



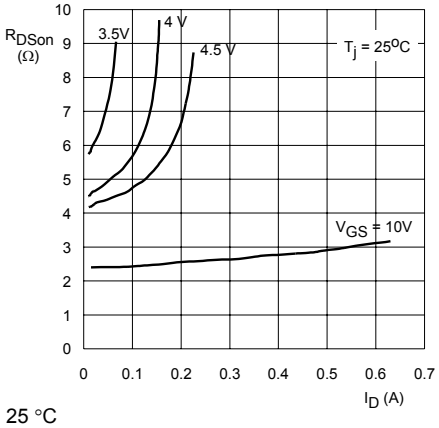
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



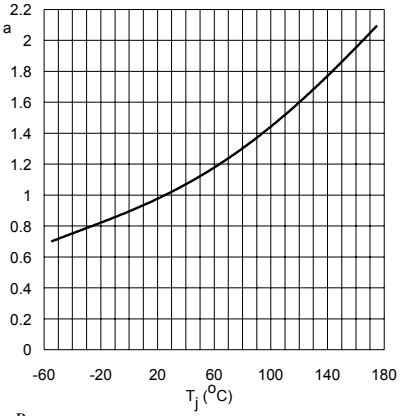
T_j = 25 °C and 150 °C; $V_{DS} \geq I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



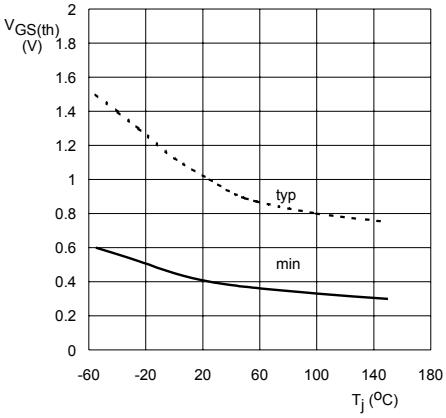
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



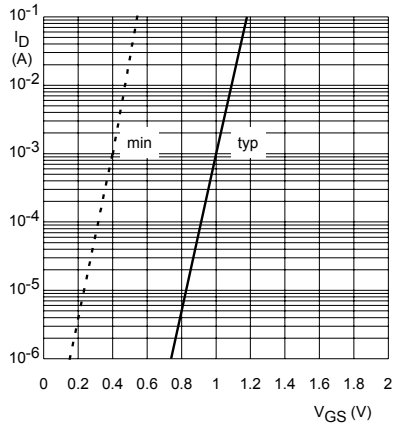
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.

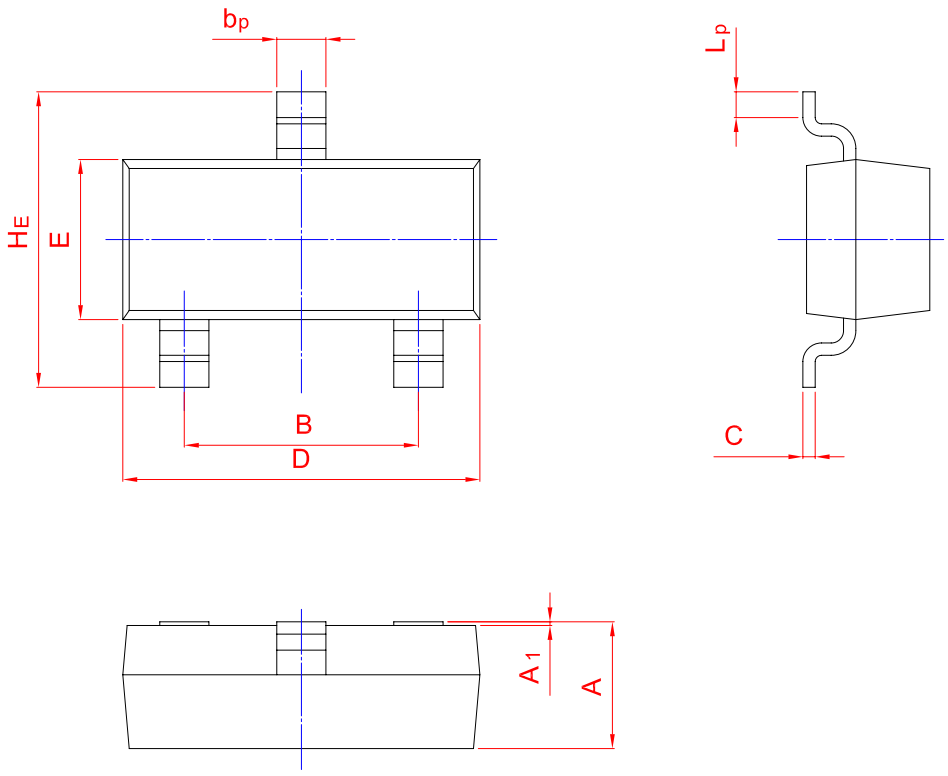


T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage.

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads **SOT-23**



UNIT	A	B	bp	C	D	E	HE	A1	Lp
mm	1.40 0.95	2.04 1.78	0.50 0.35	0.19 0.08	3.10 2.70	1.65 1.20	3.00 2.20	0.100 0.013	0.50 0.20