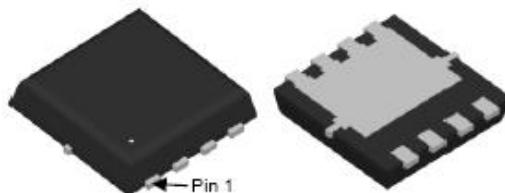


Product Summary

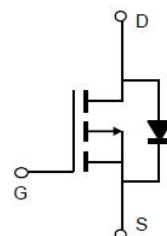
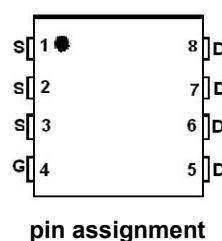
- V_{DS} -30V
- I_D -40A
- $R_{DS(ON)}$ (at $V_{GS}=-20V$) <13mohm
- $R_{DS(ON)}$ (at $V_{GS}=-10V$) <15mohm
- $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) <25mohm

Package



Top View

Bottom View



General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching

Applications

- Battery protection
- Power management
- Load switch

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
LX33F40P30	F1	40P03	5000	10000	50000	13" reel

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	V_{DS}	-30	V
Gate-source Voltage	V_{GS}	± 25	V
Drain Current <small>$T_A=25^\circ\text{C}$ @ Steady State</small>	I_D	-40	A
		-33	
Pulsed Drain Current ^A	I_{DM}	-160	A
Single Pulse Avalanche Energy @ $L=0.5\text{mH}$ ^B	E_{AS}	72	mJ
Total Power Dissipation @ $T_A=25^\circ\text{C}$ ^C	P_D	32	W
Thermal Resistance Junction-to-Ambient @ Steady State ^D	$R_{\theta JC}$	4.0	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{STG}	-55~+150	$^\circ\text{C}$



Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=-250\mu\text{A}$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=-30\text{V}, V_{\text{GS}}=0\text{V}, T_c=25^\circ\text{C}$			-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}= \pm 25\text{V}, V_{\text{DS}}=0\text{V}$			± 100	nA
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=-250\mu\text{A}$	-1.2	-1.8	-2.8	V
Static Drain-Source On-Resistance	$R_{\text{DS(ON)}}$	$V_{\text{GS}}= -20\text{V}, I_{\text{D}}=-20\text{A}$		8.6	13	$\text{m}\Omega$
		$V_{\text{GS}}= -10\text{V}, I_{\text{D}}=-15\text{A}$		9.8	15	
		$V_{\text{GS}}= -6.0\text{V}, I_{\text{D}}=-12\text{A}$		12.1	22	
		$V_{\text{GS}}= -4.5\text{V}, I_{\text{D}}=-10\text{A}$		15.5	25	
Diode Forward Voltage	V_{SD}	$I_{\text{S}}=-20\text{A}, V_{\text{GS}}=0\text{V}$			-1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{DS}}=-15\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$		2152		pF
Output Capacitance	C_{oss}			308		
Reverse Transfer Capacitance	C_{rss}			242		
Gate Resistance	R_g	$f= 1\text{MHz}$			20	Ω
Switching Parameters						
Total Gate Charge	Q_g	$V_{\text{GS}}=-10\text{V}, V_{\text{DS}}=-15\text{V}, I_{\text{D}}=-12\text{A}$		40.1		nC
Gate Source Charge	Q_{gs}			8.4		
Gate Drain Charge	Q_{gd}			8.6		
Reverse Recovery Charge	Q_{rr}	$I_{\text{F}}= -12\text{A}, di/dt=100\text{A/us}$		7.8		ns
Reverse Recovery Time	t_{rr}			18		
Turn-on Delay Time	$t_{\text{D(on)}}$	$V_{\text{GS}}=-10\text{V}, V_{\text{DD}}=-15\text{V}, I_{\text{D}}=-1\text{A}, R_{\text{GEN}}=2.5\Omega$		8		ns
Turn-on Rise Time	t_r			19		
Turn-off Delay Time	$t_{\text{D(off)}}$			75		
Turn-off Fall Time	t_f			46		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

Typical Performance Characteristics

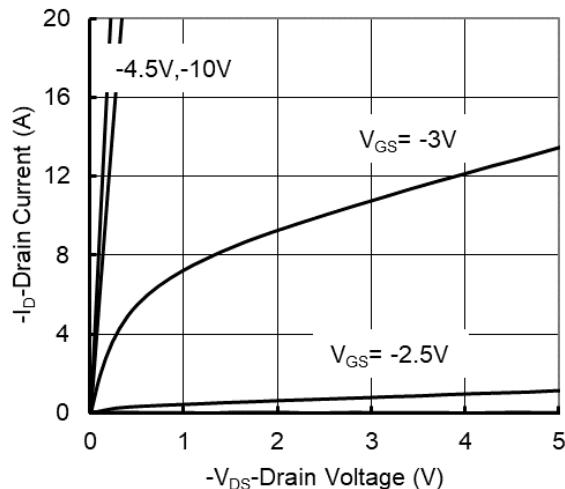


Figure 1. Output Characteristics

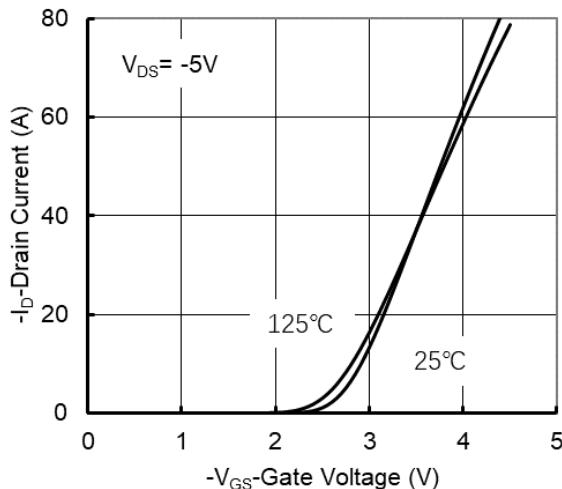


Figure 2. Transfer Characteristics

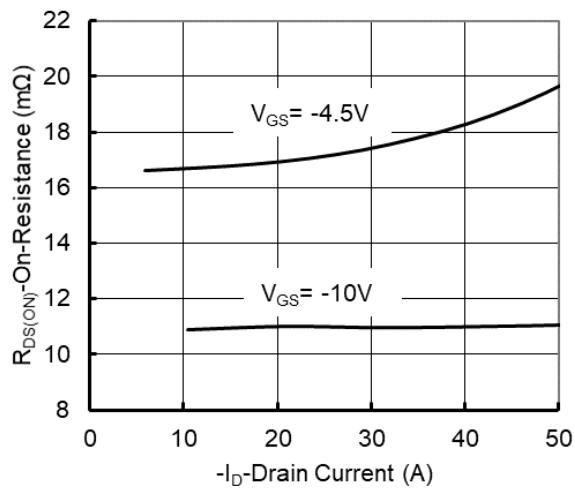


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

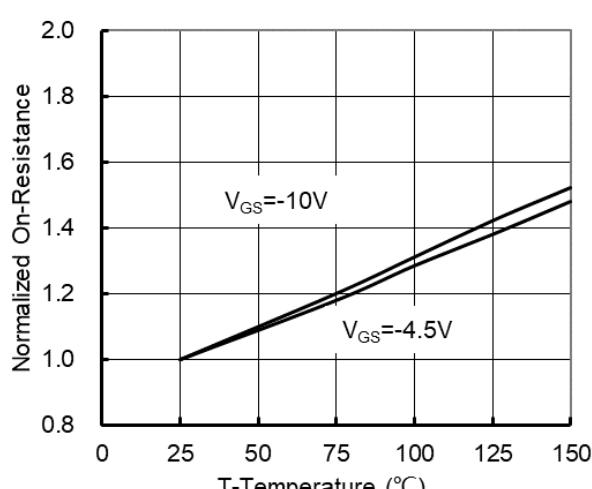


Figure 4. On-Resistance vs. Junction Temperature

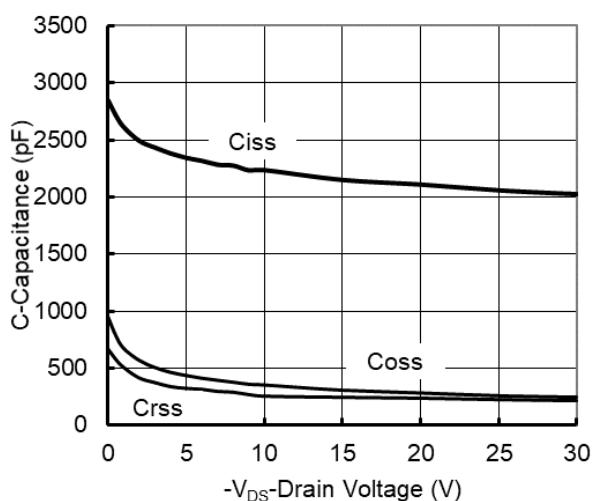


Figure 5. Capacitance Characteristics

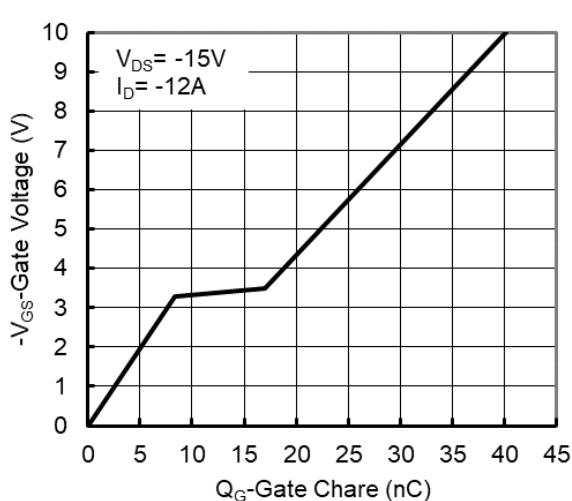
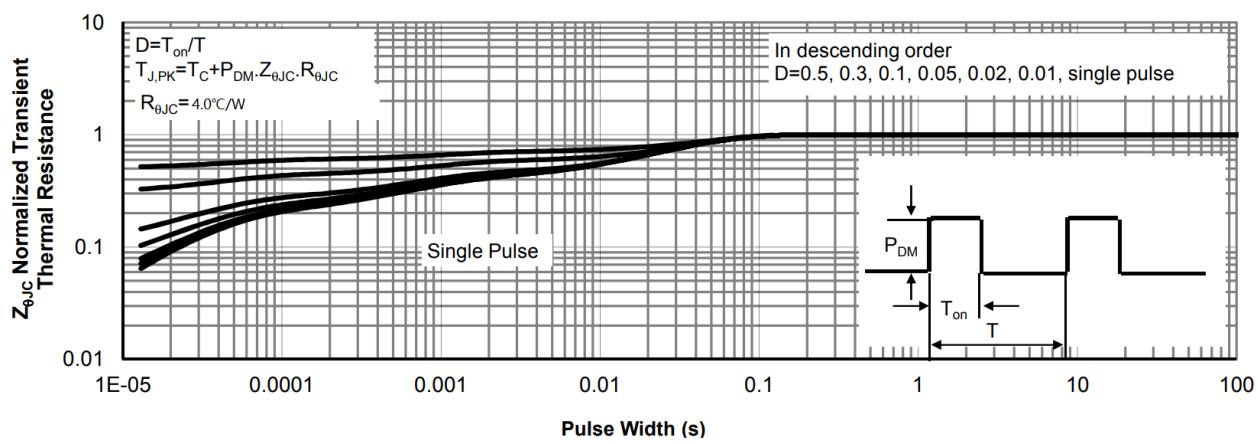
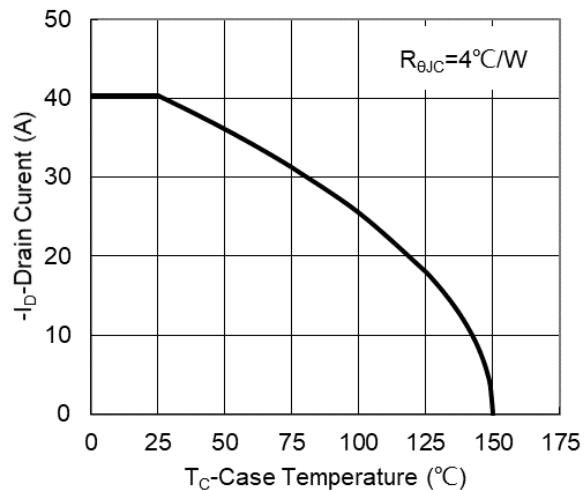
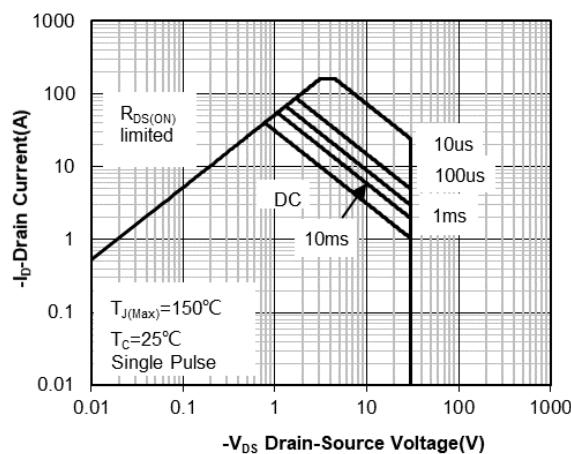
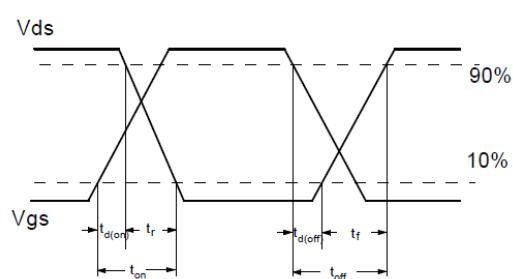
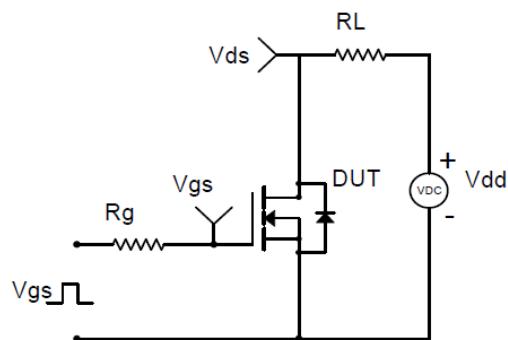
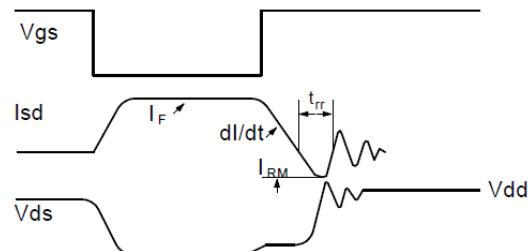
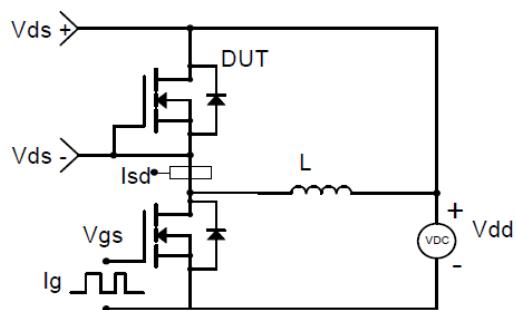


Figure 6. Gate Charge

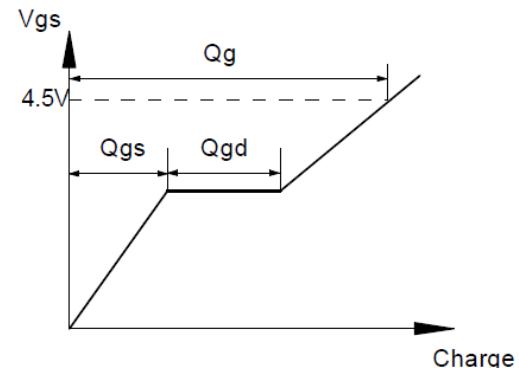
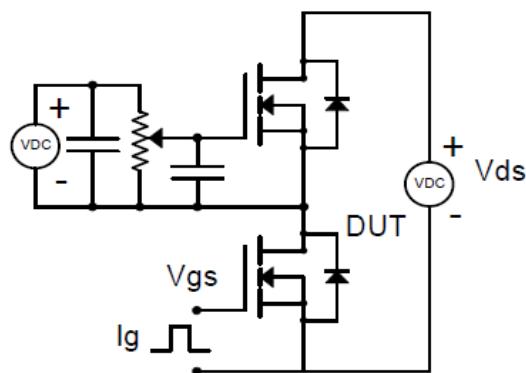




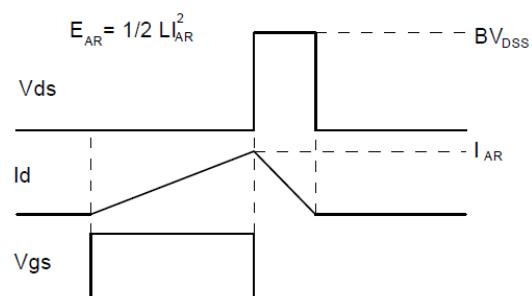
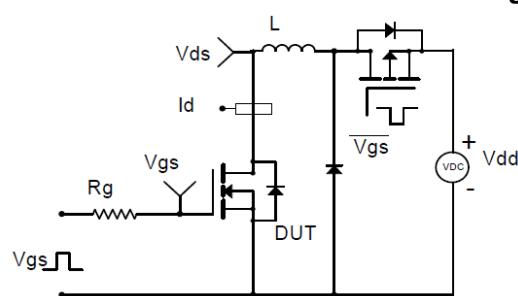
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

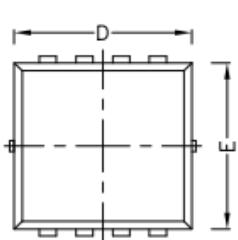


Gate Charge Test Circuit & Waveform

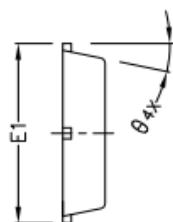


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

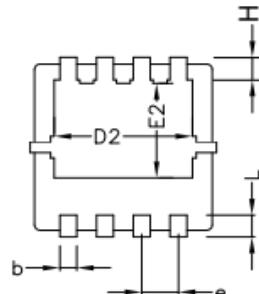
PDFN 3*3-8L Package Outline Dimensions



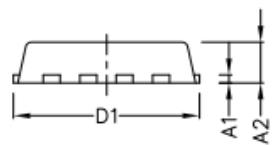
TOP VIEW



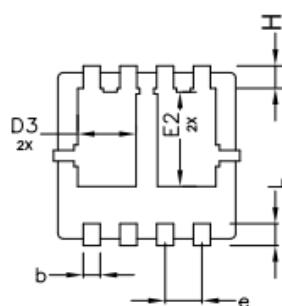
SIDE VIEW



BOTTOM VIEW
OPTION 1



SIDE VIEW



BOTTOM VIEW
OPTION 2

COMMON DIMENSIONS (UNITS OF MEASURE IS mm)			
	MIN	NORMAL	MAX
A1		0.152 BSC	
A2	0.700	0.800	0.900
b	0.250	—	0.400
D	3.050	3.150	3.250
D1	3.200	3.300	3.400
D2	2.350	2.450	2.550
D3	0.935	1.035	1.135
E1	3.200	3.300	3.400
E	2.900	3.000	3.100
E2	1.635	1.735	1.835
e		0.650 REF	
L	0.300	0.400	0.500
H	0.250	—	0.630
θ	12° TYPE		