



## FEATURES

- TrenchFET® Power MOSFET: 1.8-V Rated
- Gate-Source ESD Protected: 2000 V
- High-Side Switching
- Low On-Resistance: 0.7Ω
- Low Threshold: 0.8 V (typ)
- Fast Switching Speed: 14 ns
- S-Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

## BENEFITS

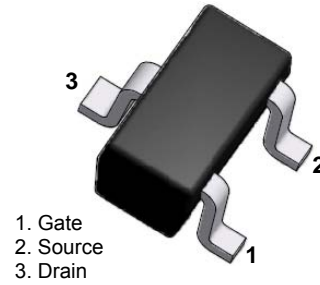
- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Battery Voltage Operation

## ORDERING INFORMATION

Device	Marking	Shipping
LX05P30C	B	3000/Tape&Reel

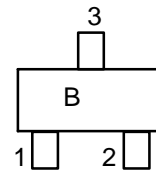
## APPLICATIONS

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones, Pagers



SOT-523

## MARKING DIAGRAM



B = Specific Device Code

## ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)

Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		V <sub>DS</sub>	-30		V
Gate-Source Voltage		V <sub>GS</sub>	±10		
Continuous Drain Current (T <sub>J</sub> = 150°C) <sup>b</sup>	T <sub>A</sub> = 25°C	I <sub>D</sub>	-500	-400	mA
	T <sub>A</sub> = 85°C		-300	-250	
Pulsed Drain Current <sup>a</sup>		I <sub>DM</sub>	-1000		
Continuous Source Current (diode conduction) <sup>b</sup>		I <sub>S</sub>	-275	-250	mW
Maximum Power Dissipation <sup>b</sup> for SOT-523	T <sub>A</sub> = 25°C	P <sub>D</sub>	175	150	
	T <sub>A</sub> = 85°C		90	80	
Maximum Power Dissipation <sup>b</sup> for SOT-523	T <sub>A</sub> = 25°C		275	250	
	T <sub>A</sub> = 85°C		160	140	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	-55 to 150		°C
Gate-Source ESD Rating (HBM, Method 3015)		ESD	2000		V

### Notes

- d. Pulse width limited by maximum junction temperature.  
e. Surface Mounted on FR4 Board.



**SPECIFICATIONS (T<sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-0.7		-1.5	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±10V		±1	±10	μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0 V			-1	μA
		V <sub>DS</sub> = -30V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85. C			-5	μA
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = -5 V, V <sub>GS</sub> = -4.5 V	-700			mA
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -300 mA		1	1.35	Ω
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -200 mA		1.6	2.1	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -250 mA		0.4		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = -150 mA, V <sub>GS</sub> = 0 V		-0.8	-1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -250 mA		1500		pC
Gate-Source Charge	Q <sub>gs</sub>			150		
Gate-Drain Charge	Q <sub>gd</sub>			450		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -10 V, R <sub>L</sub> = 47 Ω I <sub>D</sub> = -200 mA, V <sub>GEN</sub> = -4.5 V, R <sub>G</sub> = 10 Ω		5		ns
Rise Time	t <sub>r</sub>			9		
Turn-Off Delay Time	t <sub>d(off)</sub>			35		
Fall Time	t <sub>f</sub>			11		

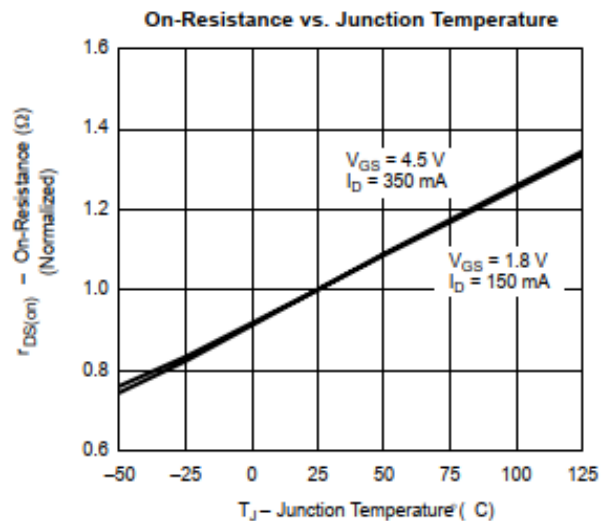
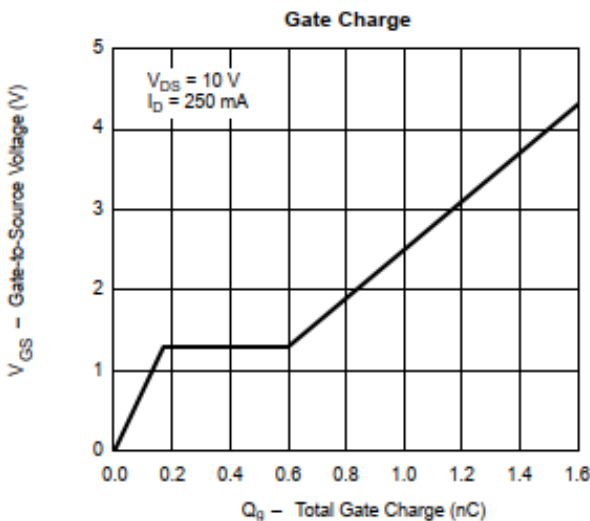
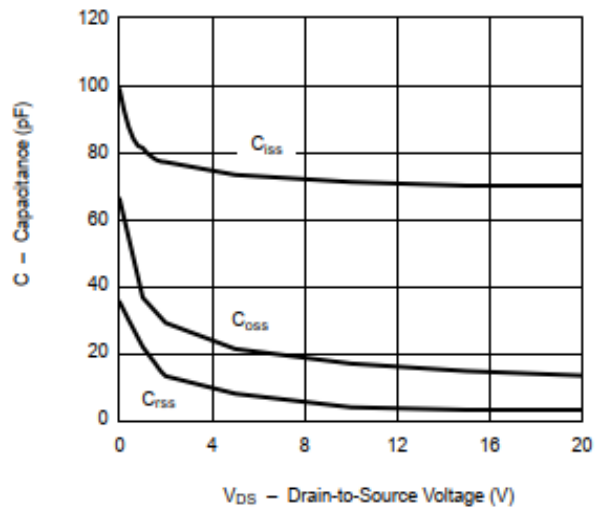
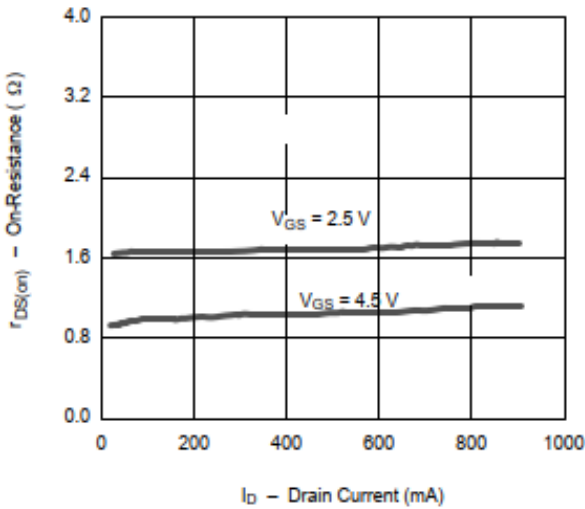
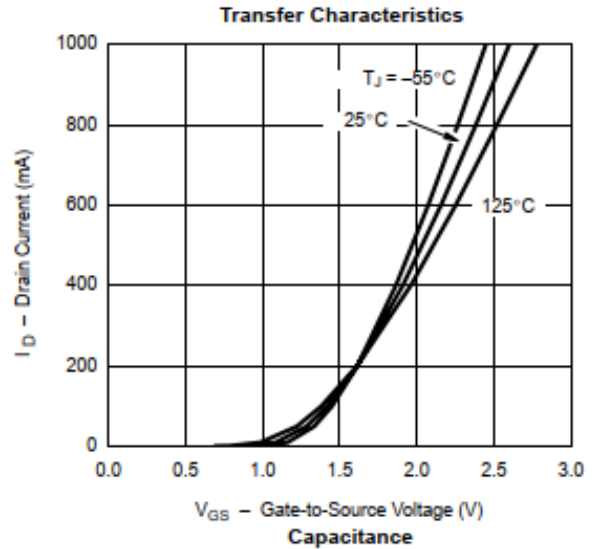
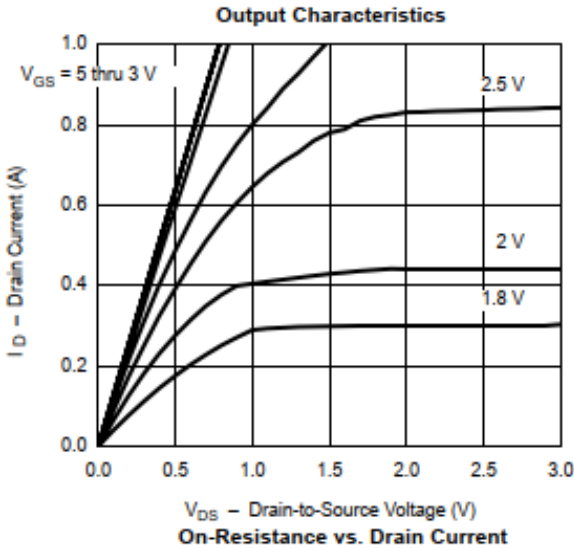
**Notes**

- a. Pulse test; pulse width ≤300μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

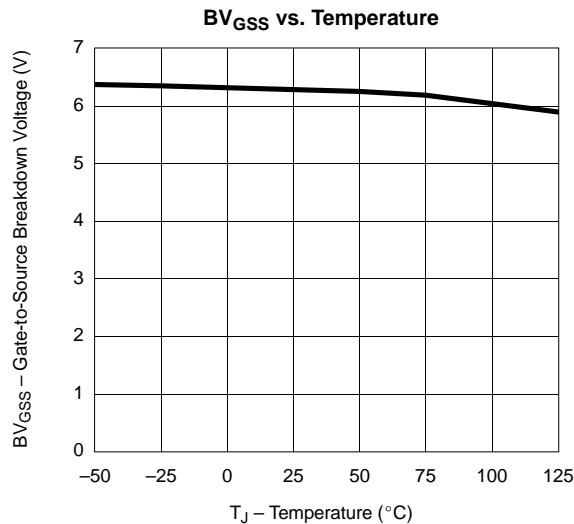
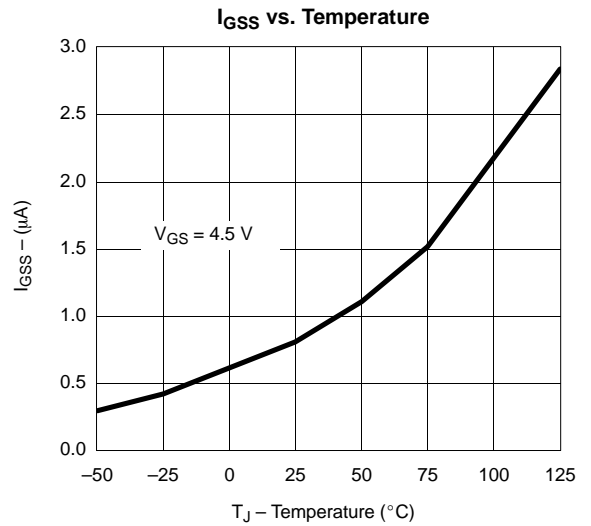
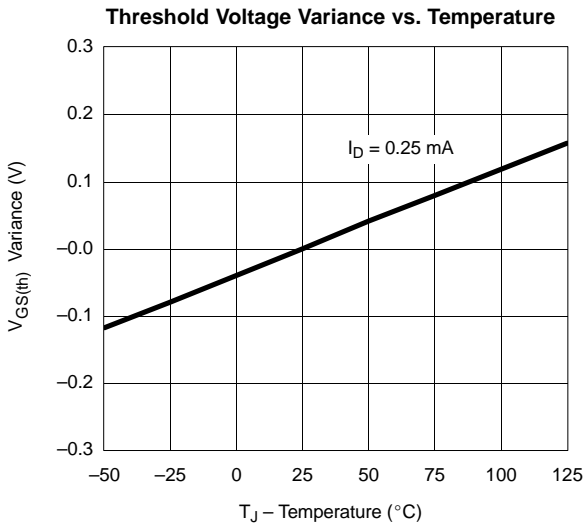
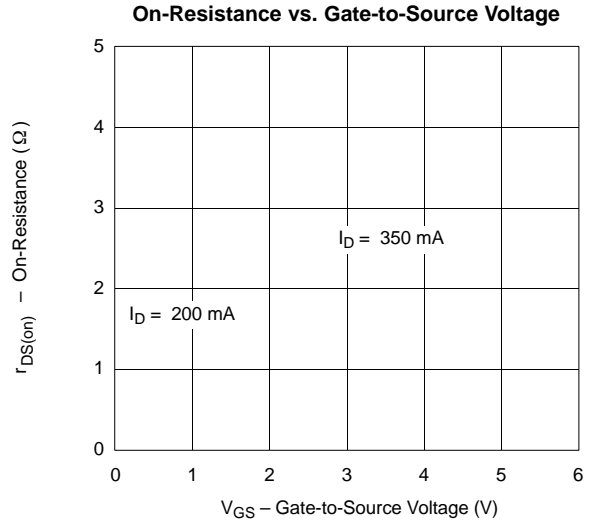
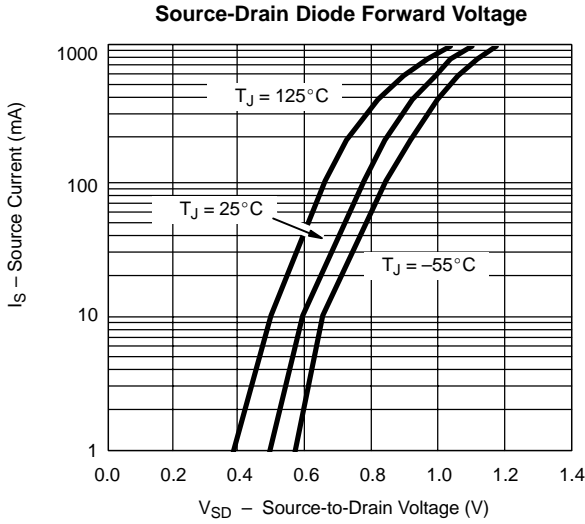


**TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C UNLESS NOTED)**

For the following graphs, p-channel negative polarities for all voltage and current values are represented as positive values.



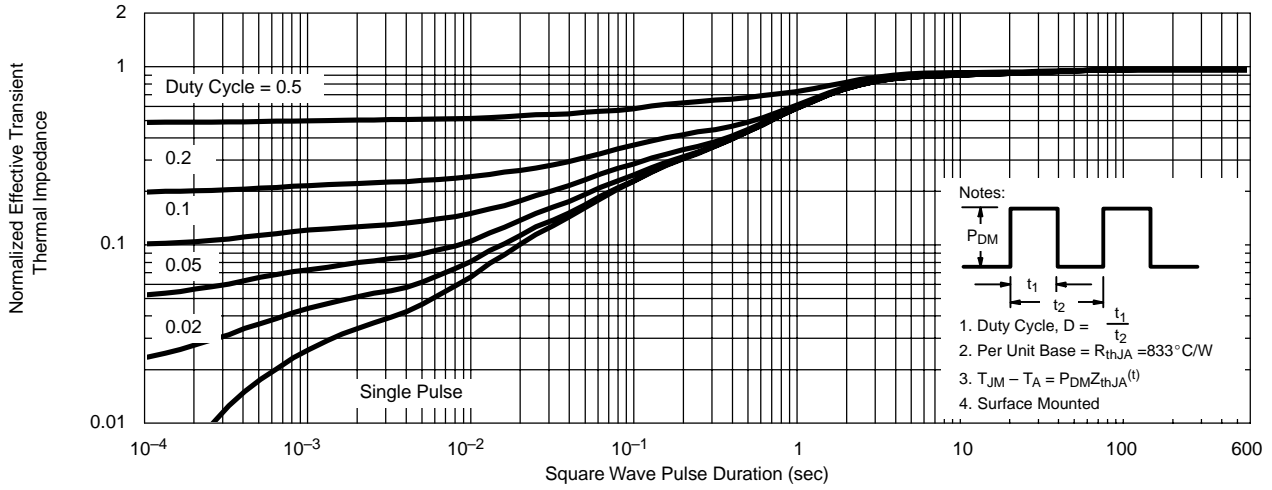
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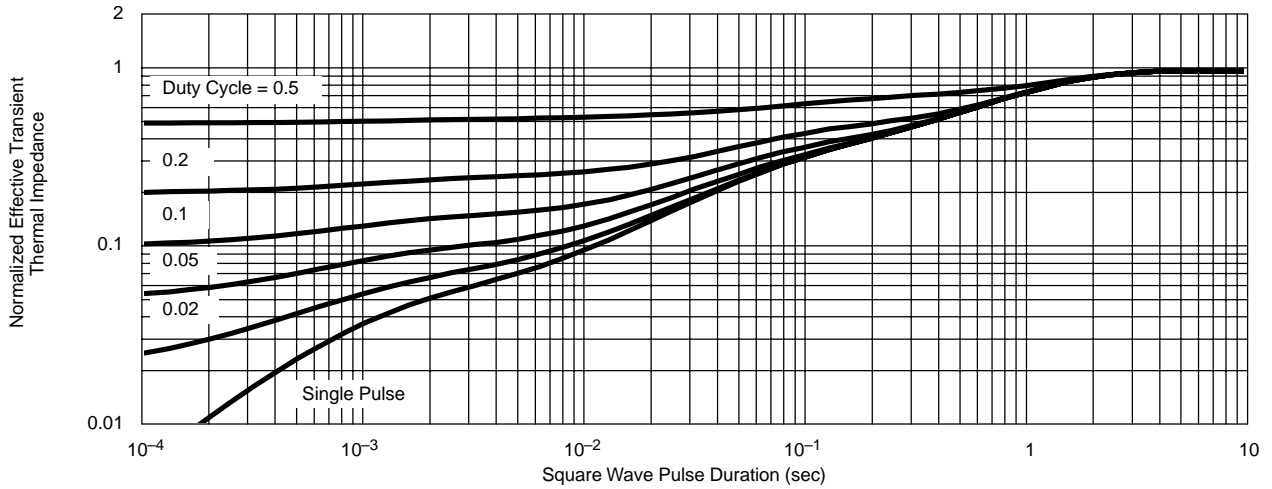


**TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C UNLESS NOTED)**

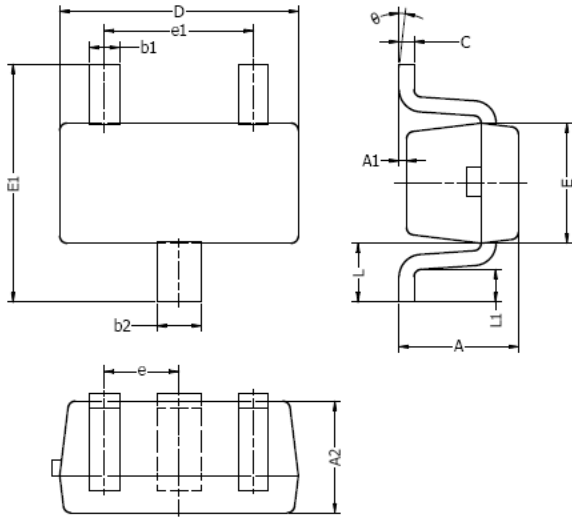
**Normalized Thermal Transient Impedance, Junction-to-Ambient (SC-75A)**



**Normalized Thermal Transient Impedance, Junction-to-Foot**

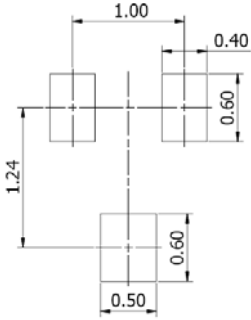


**SOT-523 Package Outline**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.90	0.028	0.035
A1	0.00	0.10	0.000	0.004
A2	0.70	0.80	0.028	0.031
b1	0.15	0.25	0.006	0.010
b2	0.25	0.35	0.010	0.014
c	0.10	0.20	0.004	0.008
D	1.50	1.70	0.059	0.067
E	0.70	0.90	0.028	0.035
E1	1.45	1.75	0.057	0.069
e	0.50 TYP.		0.020 TYP.	
e1	0.90	1.10	0.035	0.043
L	0.40 REF.		0.016 REF.	
L1	0.10	0.30	0.004	0.012
theta	0°	8°	0°	8°

**Typical Soldering Pattern:**



NOTES:  
 1. Above package outline conforms to JEITA EAIJ ED-7500A SC-75A.  
 2. Dimensions are exclusive of Burrs, Mold Flash & Tie Bar extrusions.