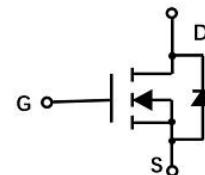
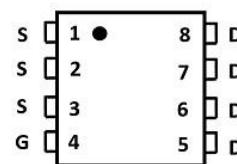
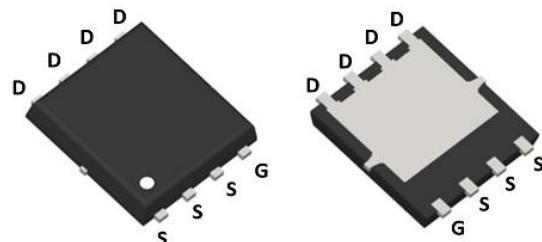


Features

- 30V,80A
 - $R_{DS(ON)}$ Typ 3.8mΩ @ $V_{GS} = 10V$
 - $R_{DS(ON)}$ Typ 6.9mΩ @ $V_{GS} = 4.5V$
- Advanced Split Gate Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

PDFN5x6-8L



Application

- Load Switch
- PWM Application
- Power management

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise specified)

| Symbol | Parameter | | Max. | Units |
|----------------|---|--------------------|-------------|--------------|
| V_{DSS} | Drain-Source Voltage | | 30 | V |
| V_{GSS} | Gate-Source Voltage | | ± 20 | V |
| I_D | Continuous Drain Current | | 80 | A |
| | $T_c = 100^\circ C$ | 46 | A | |
| I_{DM} | Pulsed Drain Current ^{note1} | | 200 | A |
| E_{AS} | Single Pulsed Avalanche Energy ^{note2} | | 150 | mJ |
| P_D | Power Dissipation | $T_c = 25^\circ C$ | 65 | W |
| R_{eJC} | Thermal Resistance, Junction to Case | | 1.92 | $^\circ C/W$ |
| T_J, T_{STG} | Operating and Storage Temperature Range | | -55 to +150 | $^\circ C$ |

Package Marking and Ordering Information

| Device Marking | Device | OUTLINE | Device Package | Reel Size | Reel (PCS) | Per Carton (PCS) |
|----------------|--------------|---------|----------------|-----------|------------|------------------|
| 80N03 | LX5060D80N30 | TAPING | PDFN5x6-8L | 13inch | 5000 | 50000 |



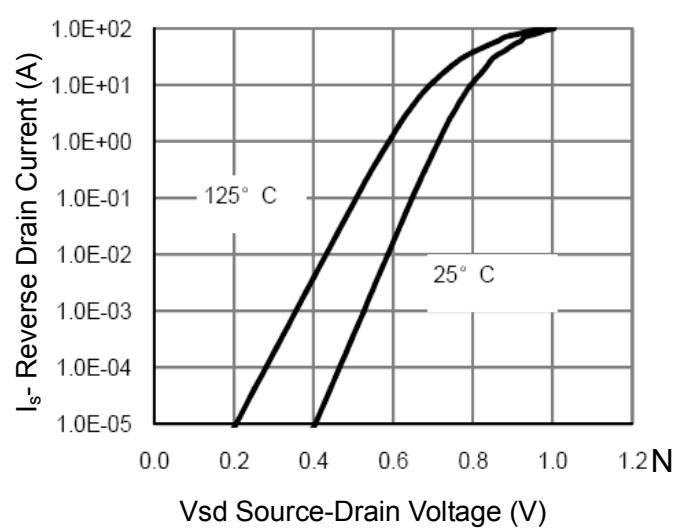
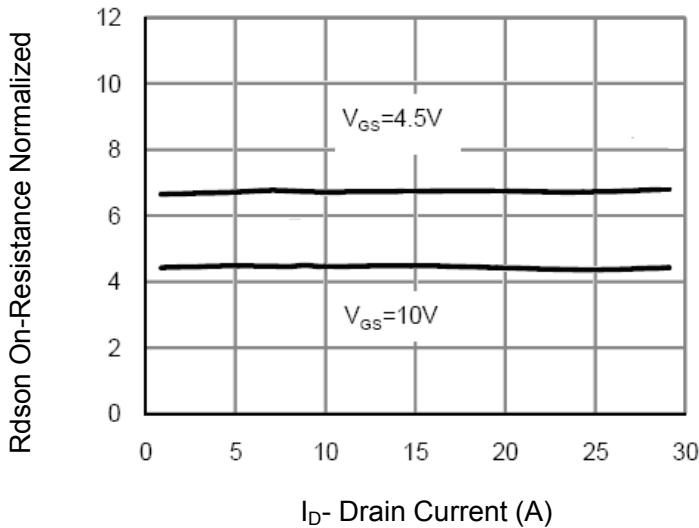
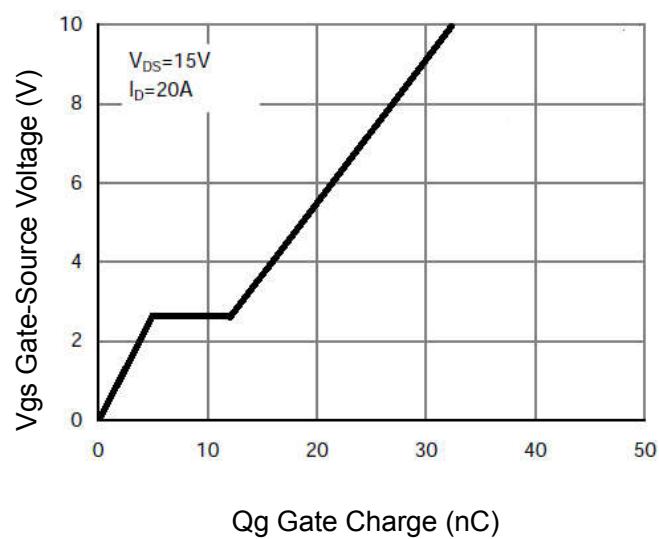
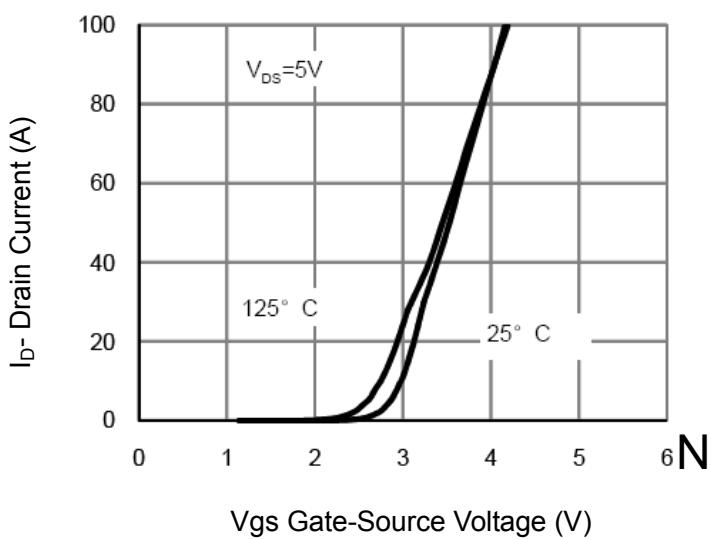
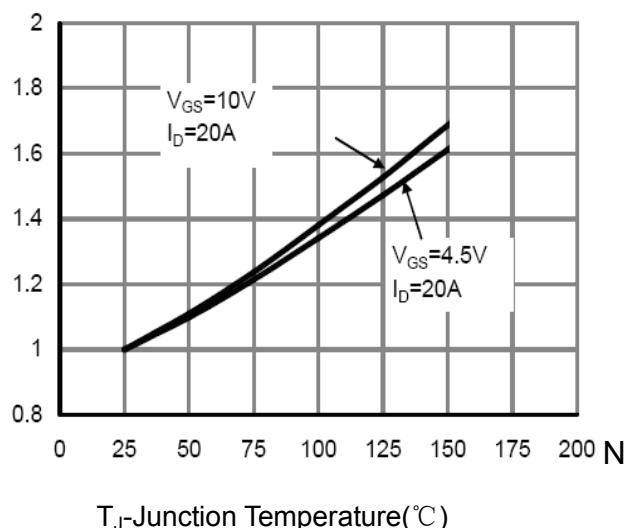
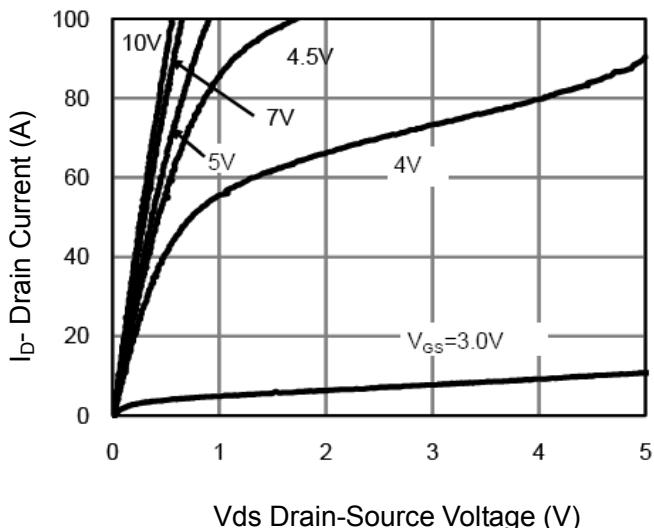
Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|--|--------------------------|---|-----|------|-----------|------------------|
| Off Characteristics | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DSS} | $V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$ | 30 | - | - | V |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{\text{DS}}=30\text{V}, V_{\text{GS}}=0\text{V}$ | - | - | 1 | μA |
| Gate-Body Leakage Current | I_{GSS} | $V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$ | - | - | ± 100 | nA |
| On Characteristics ^(Note 3) | | | | | | |
| Gate Threshold Voltage | $V_{\text{GS(th)}}$ | $V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$ | 1 | 1.6 | 2.5 | V |
| Drain-Source On-State Resistance | $R_{\text{DS(ON)}}$ | $V_{\text{GS}}=10\text{V}, I_{\text{D}}=20\text{A}$ | - | 3.8 | 5.0 | $\text{m}\Omega$ |
| | | $V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=20\text{A}$ | - | 6.9 | 11.0 | |
| Forward Transconductance | g_{FS} | $V_{\text{DS}}=5\text{V}, I_{\text{D}}=20\text{A}$ | 20 | - | - | S |
| Dynamic Characteristics ^(Note 4) | | | | | | |
| Input Capacitance | C_{iss} | $V_{\text{DS}}=15\text{V}, V_{\text{GS}}=0\text{V}, F=1.0\text{MHz}$ | - | 1400 | - | PF |
| Output Capacitance | C_{oss} | | - | 205 | - | PF |
| Reverse Transfer Capacitance | C_{rss} | | - | 177 | - | PF |
| Switching Characteristics ^(Note 4) | | | | | | |
| Turn-on Delay Time | $t_{\text{d(on)}}$ | $V_{\text{DD}}=15\text{V}, I_{\text{D}}=20\text{A}$ $V_{\text{GS}}=10\text{V}, R_{\text{GEN}}=6\Omega$ | - | 9 | - | nS |
| Turn-on Rise Time | t_r | | - | 8 | - | nS |
| Turn-Off Delay Time | $t_{\text{d(off)}}$ | | - | 28 | - | nS |
| Turn-Off Fall Time | t_f | | - | 5 | - | nS |
| Total Gate Charge | Q_g | $V_{\text{DS}}=15\text{V}, I_{\text{D}}=20\text{A},$ $V_{\text{GS}}=10\text{V}$ | - | 32.3 | - | nC |
| Gate-Source Charge | Q_{gs} | | - | 4.9 | - | nC |
| Gate-Drain Charge | Q_{gd} | | - | 6.9 | - | nC |
| Drain-Source Diode Characteristics | | | | | | |
| Diode Forward Voltage ^(Note 3) | V_{SD} | $V_{\text{GS}}=0\text{V}, I_{\text{s}}=20\text{A}$ | - | 0.85 | 1.2 | V |
| Diode Forward Current ^(Note 2) | I_s | | - | - | 65 | A |
| Reverse Recovery Time | t_{rr} | $T_J = 25^\circ\text{C}, I_F = 20\text{A}$ $dI/dt = 100\text{A}/\mu\text{s}$ ^(Note 3) | - | - | 27 | nS |
| Reverse Recovery Charge | Q_{rr} | | - | - | 20 | nC |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_j=25^\circ\text{C}, V_{\text{DD}}=15\text{V}, V_{\text{G}}=10\text{V}, L=0.5\text{mH}, R_g=25\Omega$

Typical Electrical and Thermal Characteristics (Curves)



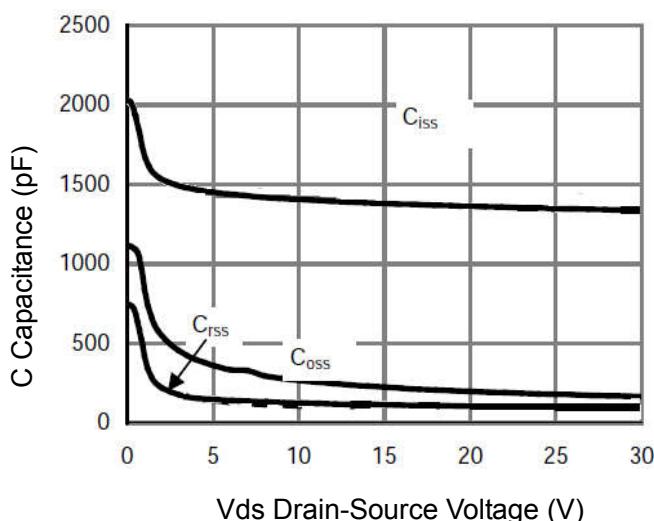


Figure 7 Capacitance vs Vds

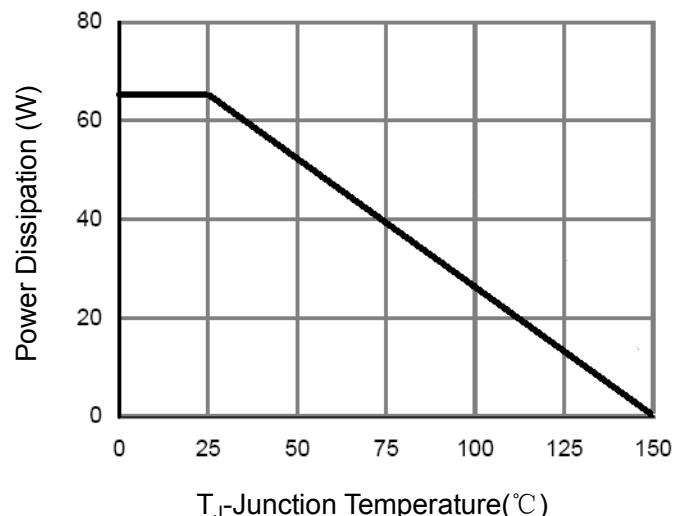


Figure 9 Power De-rating

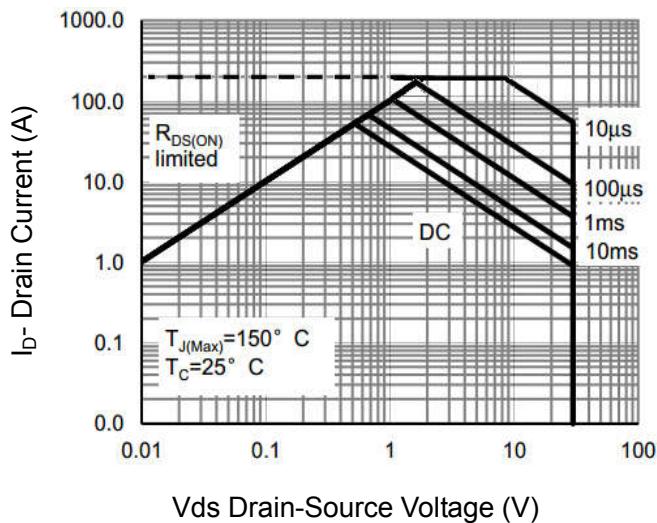


Figure 8 Safe Operation Area

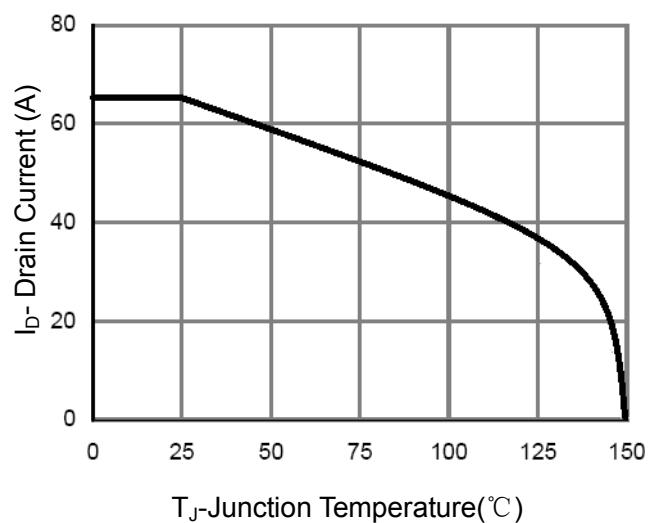


Figure 10 ID Current- Junction Temperature

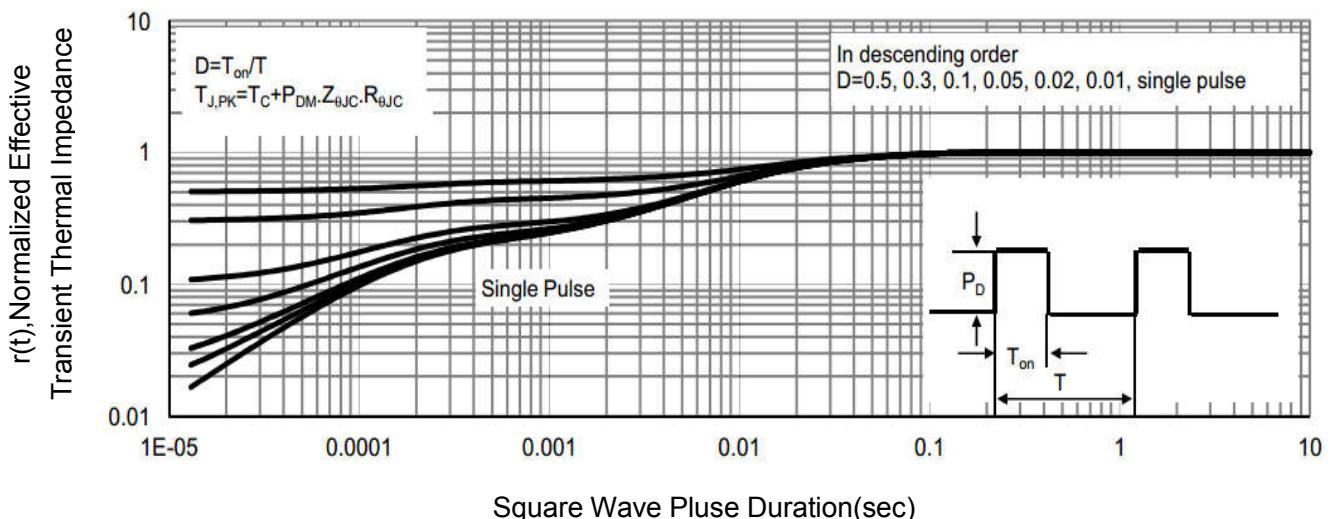


Figure 11 Normalized Maximum Transient Thermal Impedance

Test Circuit

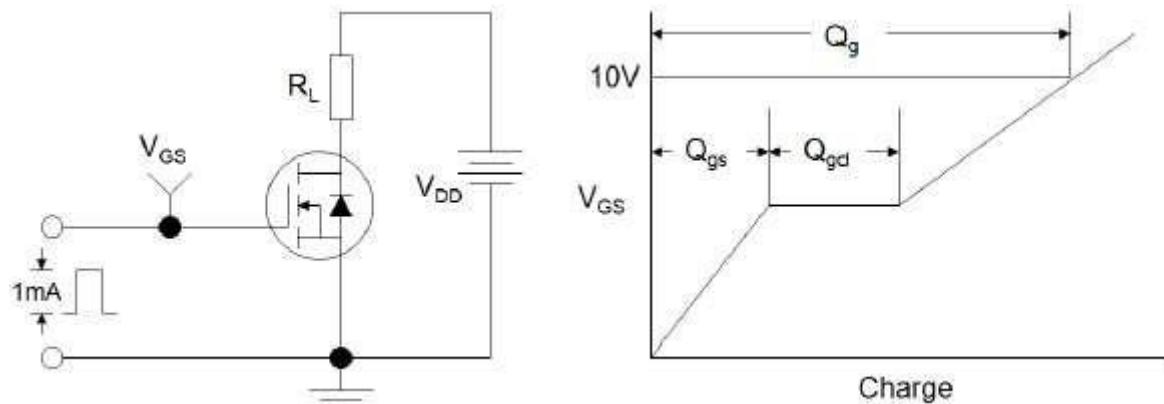


Figure 1:Gate Charge Test Circuit & Waveform

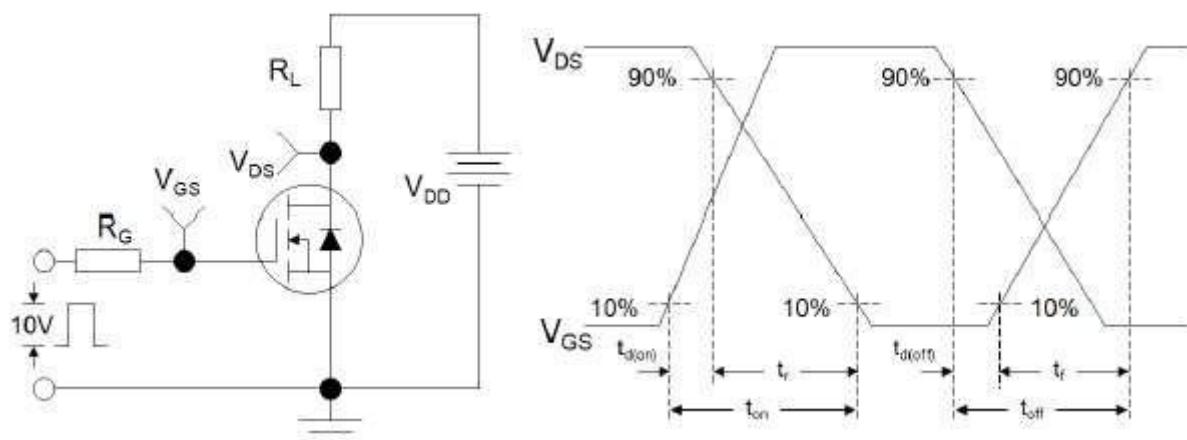


Figure 2: Resistive Switching Test Circuit & Waveforms

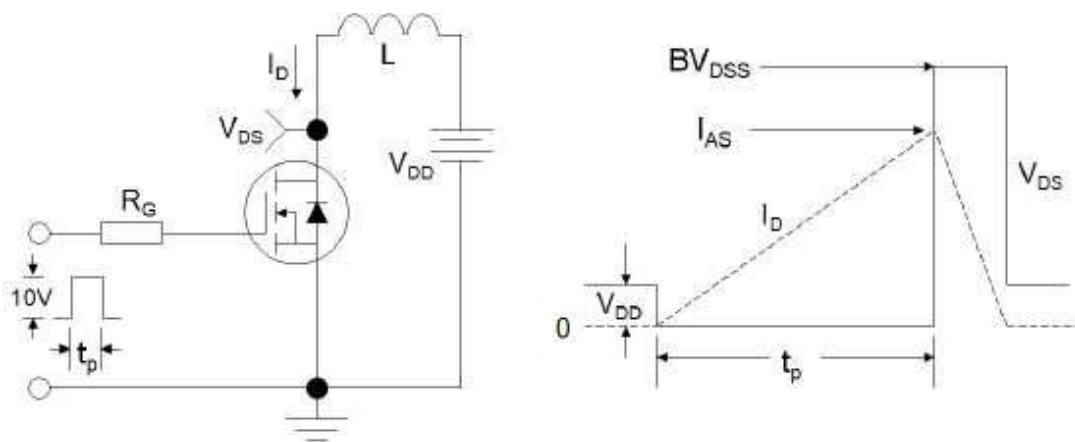
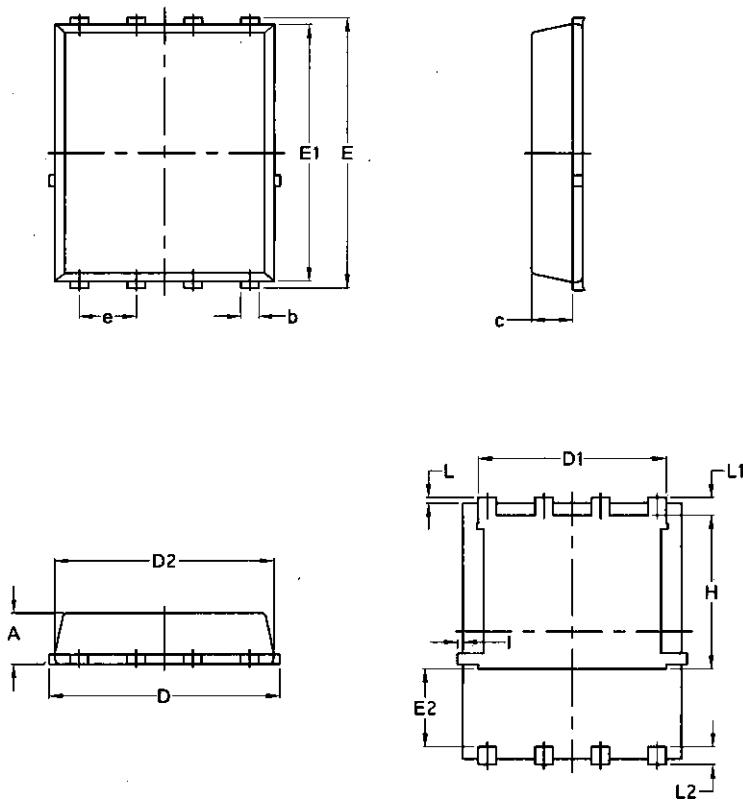


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

Package Mechanical Data-PDFN5*6-8L-JQ Single



| Symbol | Common | | | |
|--------|----------|--------|----------|--------|
| | mm | | Inch | |
| | Mim | Max | Min | Max |
| A | 1.03 | 1.17 | 0.0406 | 0.0461 |
| b | 0.34 | 0.48 | 0.0134 | 0.0189 |
| c | 0.824 | 0.0970 | 0.0324 | 0.082 |
| D | 4.80 | 5.40 | 0.1890 | 0.2126 |
| D1 | 4.11 | 4.31 | 0.1618 | 0.1697 |
| D2 | 4.80 | 5.00 | 0.1890 | 0.1969 |
| E | 5.95 | 6.15 | 0.2343 | 0.2421 |
| E1 | 5.65 | 5.85 | 0.2224 | 0.2303 |
| E2 | 1.60 | / | 0.0630 | / |
| e | 1.27 BSC | | 0.05 BSC | |
| L | 0.05 | 0.25 | 0.0020 | 0.0098 |
| L1 | 0.38 | 0.50 | 0.0150 | 0.0197 |
| L2 | 0.38 | 0.50 | 0.0150 | 0.0197 |
| H | 3.30 | 3.50 | 0.1299 | 0.1378 |
| I | / | 0.18 | / | 0.0070 |