

FEATURE

- Surface Mount Package
- Low $R_{DS(on)}$
- Operated at Low Logic Level Gate Drive
- ESD Protected Gate
- Including a N-ch LX3134K and a P-ch LX3139K (independently) In a Package

APPLICATION

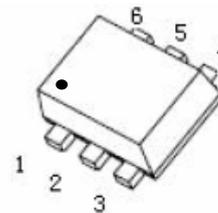
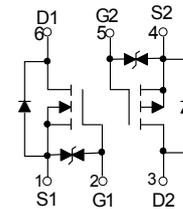
- Load/ Power Switching
- Interfacing Switching
- Battery Management for Ultra Small Portable Electronics
- Logic Level Shift

MARKING

- MARKING:49K

N Channel +P Channel MOSFET

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	I_D
20V	380mΩ@ 4.5V	0.75A
	450mΩ@ 2.5V	
	800mΩ@ 1.8V	
-20V	520mΩ@-4.5V	-0.66A
	700mΩ@-2.5V	
	950mΩ(TYP)@-1.8V	



SOT-563

ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
N-MOSFET			
Drain-Source Voltage	V_{DS}	20	V
Typical Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current (note 1)	I_D	0.75	A
Pulsed Drain Current ($t_p=10\mu\text{s}$)	I_{DM}	1.8	A
P-MOSFET			
Drain-Source Voltage	V_{DS}	-20	V
Typical Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current (note 1)	I_D	-0.66	A
Pulsed Drain Current ($t_p=10\mu\text{s}$)	I_{DM}	-1.2	A
Temperature and Thermal Resistance			
Thermal Resistance from Junction to Ambient (note 1)	$R_{\theta JA}$	833	$^\circ\text{C}/\text{W}$
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55~+150	$^\circ\text{C}$
Lead Temperature for Soldering Purposes(1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$



MOSFET ELECTRICAL CHARACTERISTICS

N-ch MOSFET ELECTRICAL CHARACTERISTICS(Ta=25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
STATIC CHARACTERISTICS						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	20			V
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 20V, V_{GS} = 0V$			1	μA
Gate-body leakage current	I_{GSS}	$V_{GS} = \pm 10V, V_{DS} = 0V$			± 20	μA
Gate threshold voltage (note 2)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.35		1.1	V
Drain-source on-resistance(note 2)	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 0.65A$			380	$m\Omega$
		$V_{GS} = 2.5V, I_D = 0.55A$			450	$m\Omega$
		$V_{GS} = 1.8V, I_D = 0.45A$			800	$m\Omega$
Forward tranconductance(note 2)	g_{FS}	$V_{DS} = 10V, I_D = 0.8A$		1.6		S
Diode forward voltage	V_{SD}	$I_S = 0.15A, V_{GS} = 0V$			1.2	V
DYNAMIC CHARACTERISTICS (note 4)						
Input Capacitance	C_{iss}	$V_{DS} = 16V, V_{GS} = 0V, f = 1MHz$		79	120	pF
Output Capacitance	C_{oss}			13	20	pF
Reverse Transfer Capacitance	C_{rss}			9	15	pF
SWITCHING CHARACTERISTICS (note 3,4)						
Turn-on delay time	$t_{d(on)}$	$V_{GS} = 4.5V, V_{DS} = 10V, I_D = 500mA, R_{GEN} = 10\Omega$		6.7		ns
Turn-on rise time	t_r			4.8		ns
Turn-off delay time	$t_{d(off)}$			17.3		ns
Turn-off fall time	t_f			7.4		ns

P-ch MOSFET ELECTRICAL CHARACTERISTICS(Ta=25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
STATIC CHARACTERISTICS						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
Zero gate voltage drain current	I_{DSS}	$V_{DS} = -20V, V_{GS} = 0V$			-1	μA
Gate-body leakage current	I_{GSS}	$V_{GS} = \pm 10V, V_{DS} = 0V$			± 20	μA
Gate threshold voltage (note 2)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.35		-1.1	V
Drain-source on-resistance(note 2)	$R_{DS(on)}$	$V_{GS} = -4.5V, I_D = -1A$		270	520	$m\Omega$
		$V_{GS} = -2.5V, I_D = -0.8A$		320	700	$m\Omega$
		$V_{GS} = -1.8V, I_D = -0.5A$		950		$m\Omega$
Forward tranconductance(note 2)	g_{FS}	$V_{DS} = -10V, I_D = -0.54A$		1.2		S
Diode forward voltage	V_{SD}	$I_S = -0.5A, V_{GS} = 0V$			-1.2	V
DYNAMIC CHARACTERISTICS (note 4)						
Input Capacitance	C_{iss}	$V_{DS} = -16V, V_{GS} = 0V, f = 1MHz$		113	170	pF
Output Capacitance	C_{oss}			15	25	pF
Reverse Transfer Capacitance	C_{rss}			9	15	pF
SWITCHING CHARACTERISTICS (note 3,4)						
Turn-on delay time	$t_{d(on)}$	$V_{GS} = -4.5V, V_{DS} = -10V, I_D = -200mA, R_{GEN} = 10\Omega$		9		ns
Turn-on rise time	t_r			5.8		ns
Turn-off delay time	$t_{d(off)}$			32.7		ns
Turn-off fall time	t_f			20.3		ns

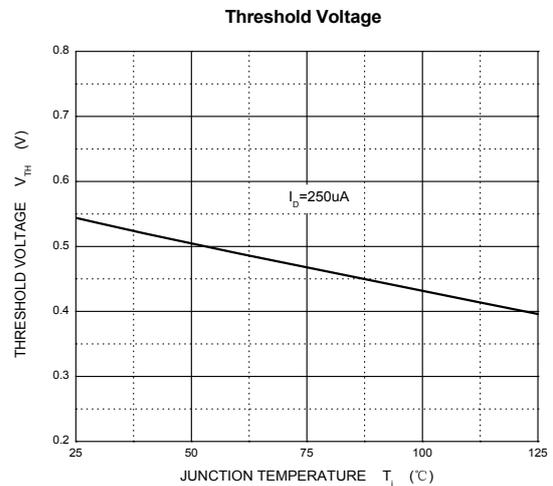
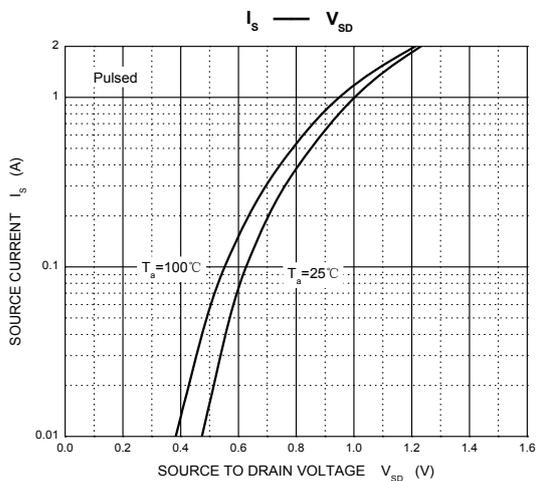
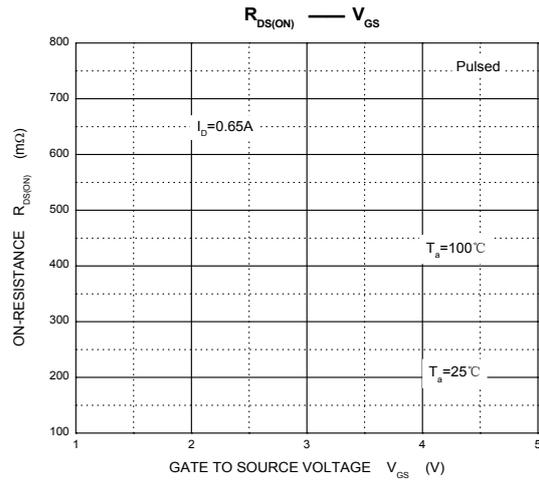
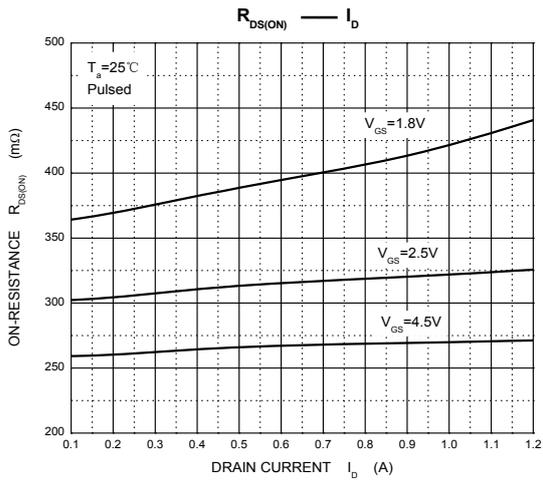
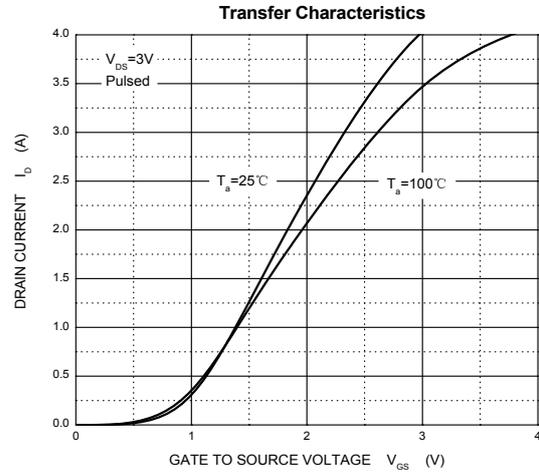
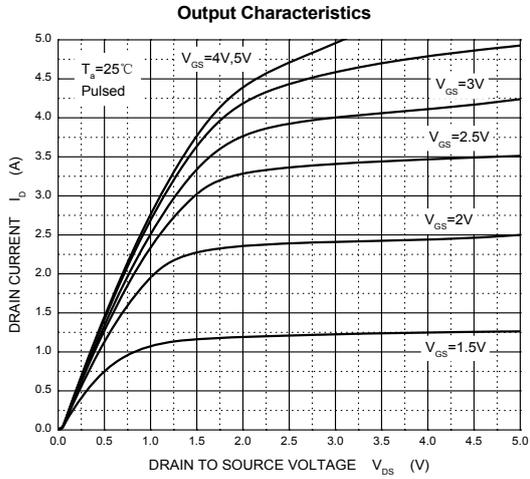
Notes :

- 1.Surface mounted on FR4 board using the minimum recommended pad size.
2. Pulse Test : Pulse width=300 μs , duty cycle $\leq 2\%$.
3. Switching characteristics are independent of operating junction temperature.
4. Garanted by design, not subject to producing.



Typical Characteristics

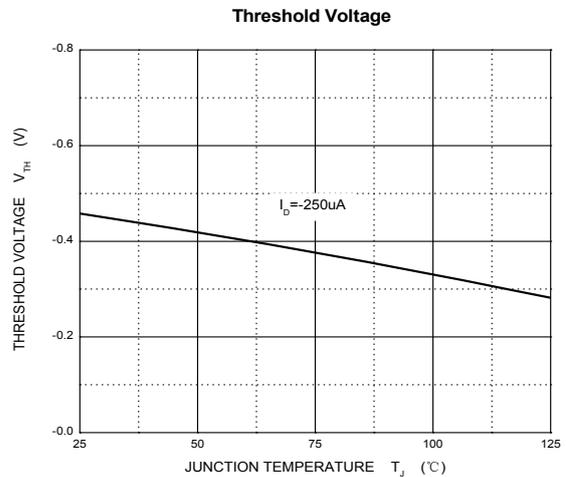
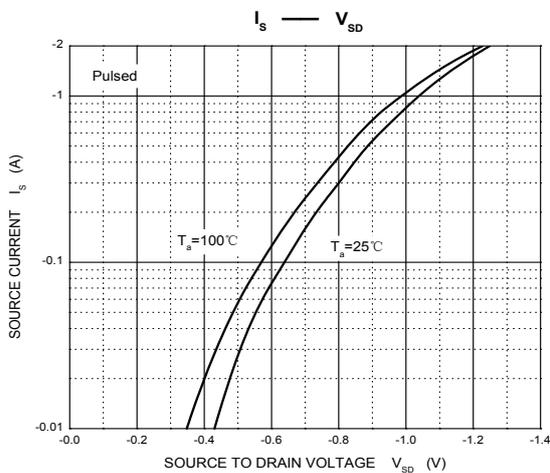
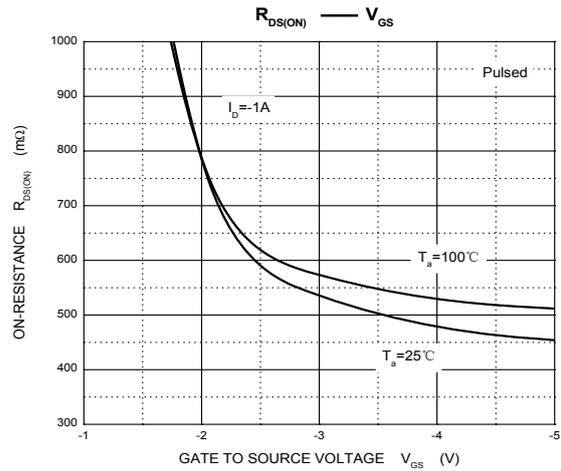
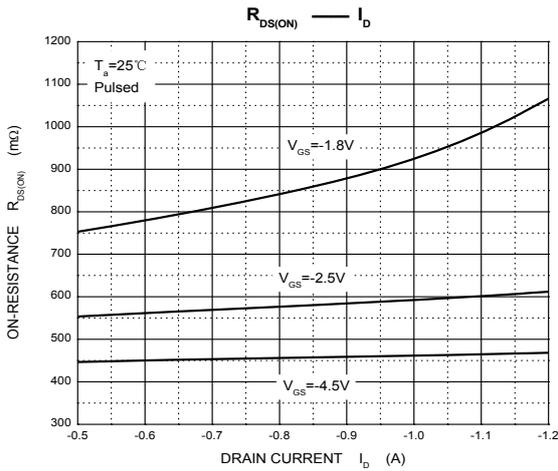
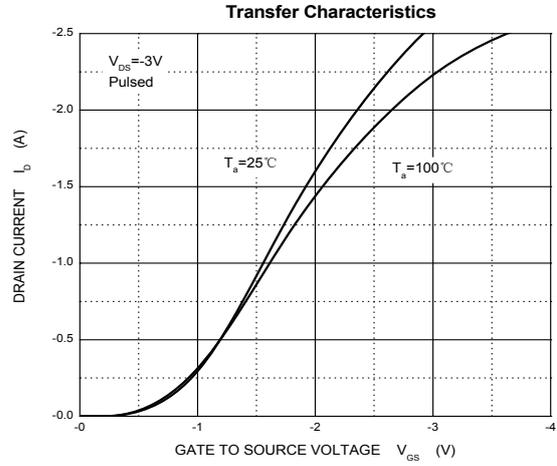
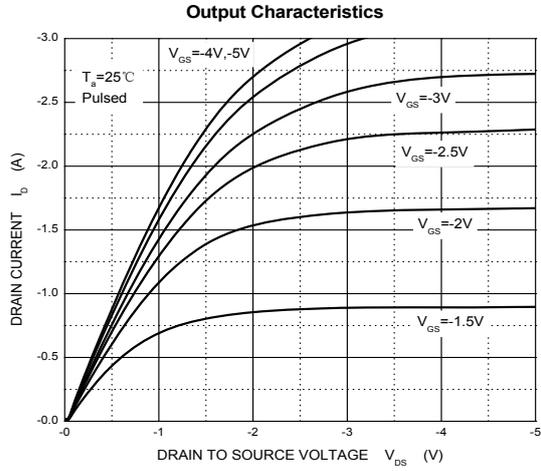
N-Channel MOS



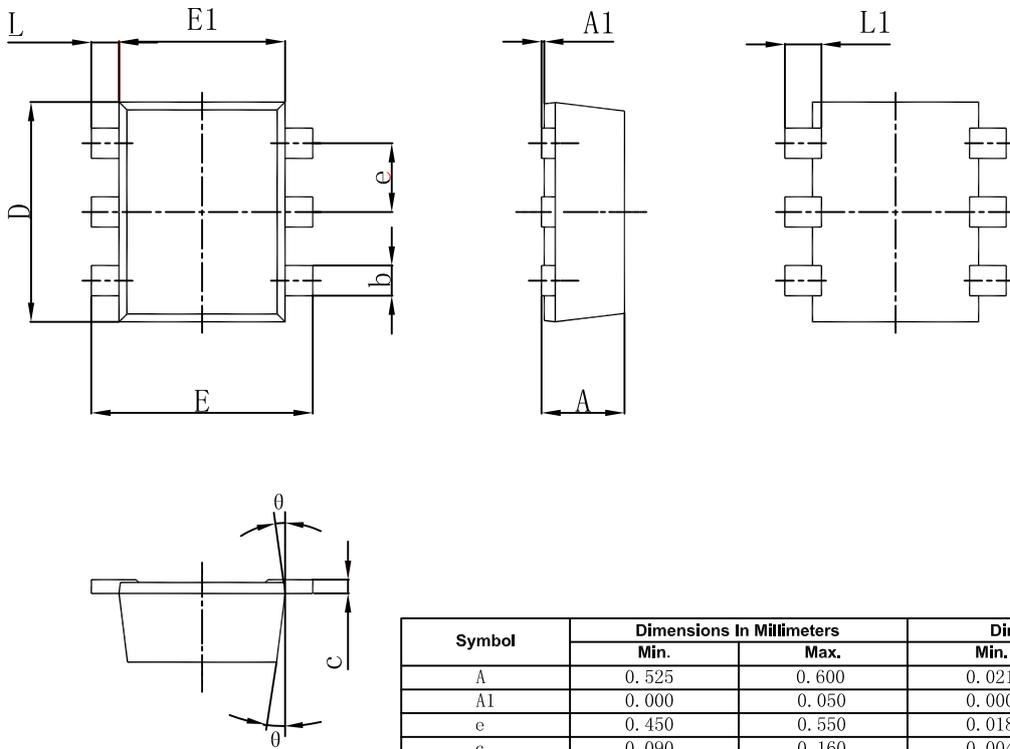


Typical Characteristics

P-Channel MOS

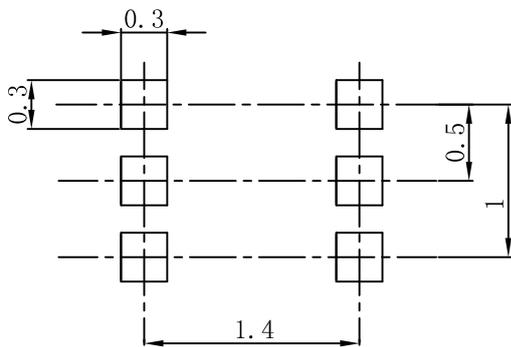


SOT-563 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.525	0.600	0.021	0.024
A1	0.000	0.050	0.000	0.002
e	0.450	0.550	0.018	0.022
c	0.090	0.160	0.004	0.006
D	1.500	1.700	0.059	0.067
b	0.170	0.270	0.007	0.011
E1	1.100	1.300	0.043	0.051
E	1.500	1.700	0.059	0.067
L	0.100	0.300	0.004	0.012
L1	0.200	0.400	0.008	0.016
θ	7 °REF.		7 °REF.	

SOT-563 Suggested Pad Layout



- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.05\text{mm}$.
 3. The pad layout is for reference purposes only.