



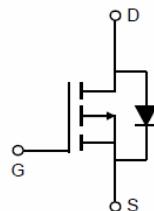
## Description

The LX33F40P20 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

## General Features

- $V_{DS} = -20V, I_D = -40A$
- $R_{DS(ON)} \text{ Typ } = 6.6m\Omega @ V_{GS} = -4.5V$
- $R_{DS(ON)} \text{ Typ } = 8.5m\Omega @ V_{GS} = -2.5V$
- High density cell design for ultra low  $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation

## Schematic diagram



## Package

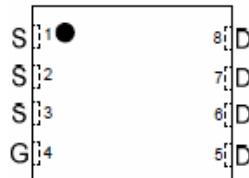


DFN 3.3x3.3 EP top view

## Application

- Load switch
- Battery protection

## Pin Assignment



## Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
7421	LX33F40P20	DFN 3.3x3.3 EP	-	-	-

## Absolute Maximum Ratings (TC=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Drain Current-Continuous	$I_D$	-40	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D (100^\circ C)$	-30	A
Pulsed Drain Current	$I_{DM}$	-170	A
Maximum Power Dissipation	$P_D$	70	W
Derating factor		0.58	W/ $^\circ C$
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

## Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	1.6	$^\circ C/W$
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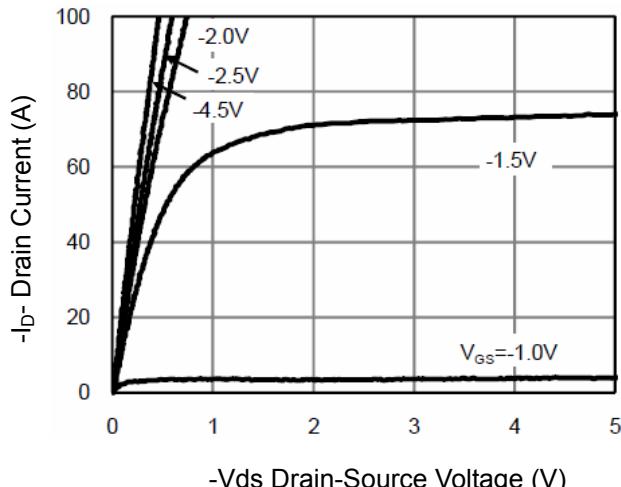
Electrical Characteristics ( $T_c=25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage $V_{GS}=0\text{V}, I_D=-250\mu\text{A}$			-20	-	-	V
Zero Gate Voltage Drain Current $V_{DS}=-16\text{V}, V_{GS}=0\text{V}$			-	-	1	$\mu\text{A}$
Gate-Body Leakage Current $V_{GS}=\pm 12\text{V}, V_{DS}=0\text{V}$			-	-	$\pm 100$	nA
<b>On Characteristics</b> <small>(Note 3)</small>						
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-0.4	-0.6	-1.0	V
Drain-Source On-State Resistance	$R_{DS(\text{ON})}$	$V_{GS}=-4.5\text{V}, I_D=-15\text{A}$	-	6.6	8.5	$\text{m}\Omega$
		$V_{GS}=-2.5\text{V}, I_D=-10\text{A}$	-	8.5	12	
Forward Transconductance	$g_{FS}$	$V_{DS}=-5\text{V}, I_D=-20\text{A}$	80	-	-	S
<b>Dynamic Characteristics</b> <small>(Note 4)</small>						
Input Capacitance	$C_{iss}$	$V_{DS}=-10\text{V}, V_{GS}=0\text{V}, F=1.0\text{MHz}$	-	3500	-	PF
Output Capacitance	$C_{oss}$		-	577	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	445	-	PF
<b>Switching Characteristics</b> <small>(Note 4)</small>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-10\text{V}, R_{GEN}=3\Omega$ $V_{GS}=-4.5\text{V}, R_L=0.5\Omega$	-	18	-	nS
Turn-on Rise Time	$t_r$		-	42	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	85	-	nS
Turn-Off Fall Time	$t_f$		-	23	-	nS
Total Gate Charge	$Q_g$		-	55	-	nC
Gate-Source Charge	$Q_{gs}$	$V_{DS}=-10\text{V}, I_D=-20\text{A}, V_{GS}=-4.5\text{V}$	-	10	-	nC
Gate-Drain Charge	$Q_{gd}$		-	15	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <small>(Note 3)</small>	$V_{SD}$	$V_{GS}=0\text{V}, I_S=-20\text{A}$	-	-	-1.2	V
Diode Forward Current <small>(Note 2)</small>	$I_S$		-	-	-45	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}, IF = -10\text{A}$ $di/dt = 100\text{A}/\mu\text{s}$ <small>(Note 3)</small>	-	47	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	53	-	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

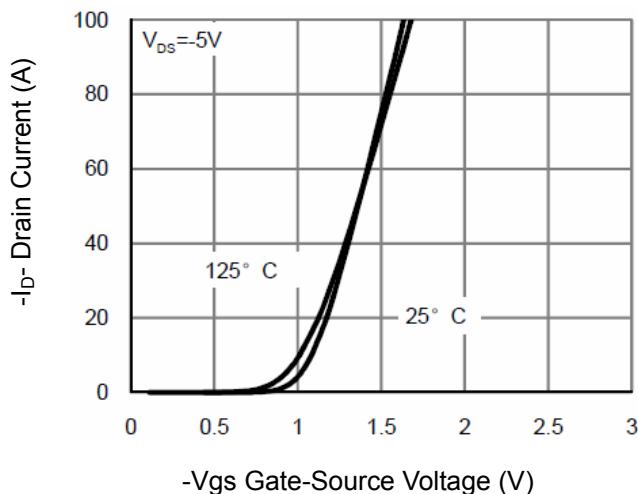
## Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

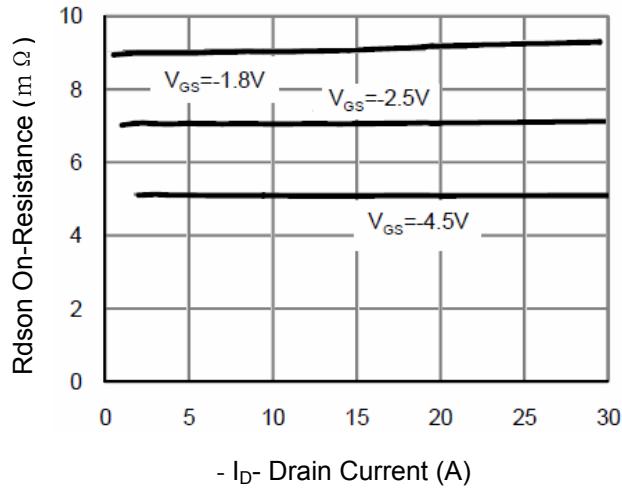
## Typical Electrical and Thermal Characteristics (Curves)



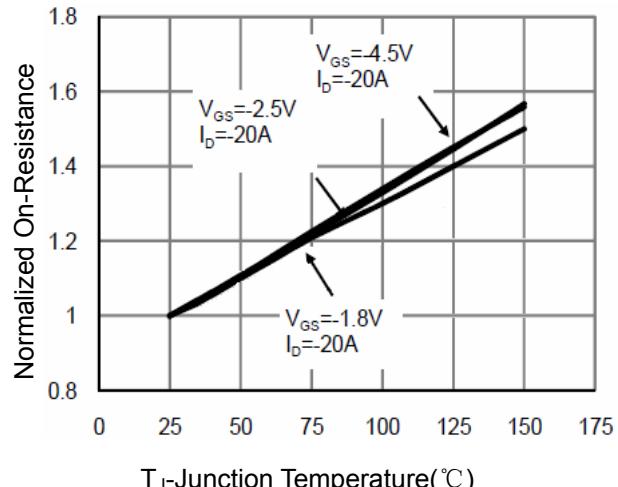
**Figure 1 Output Characteristics**



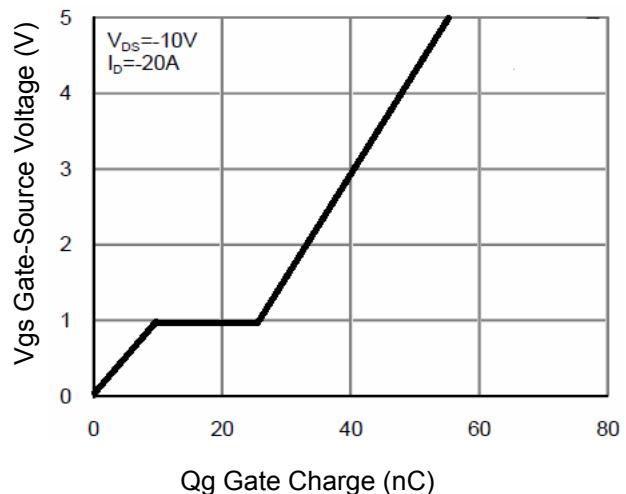
**Figure 2 Transfer Characteristics**



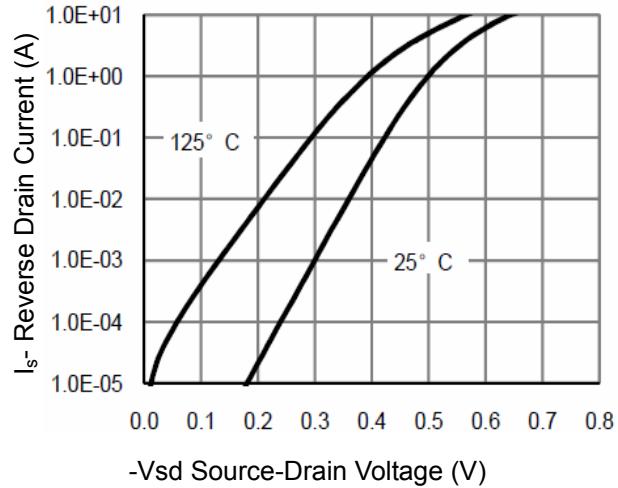
**Figure 3 Rdson- Drain Current**



**Figure 4 Rdson-Junction Temperature**



**Figure 5 Gate Charge**



**Figure 6 Source- Drain Diode Forward**

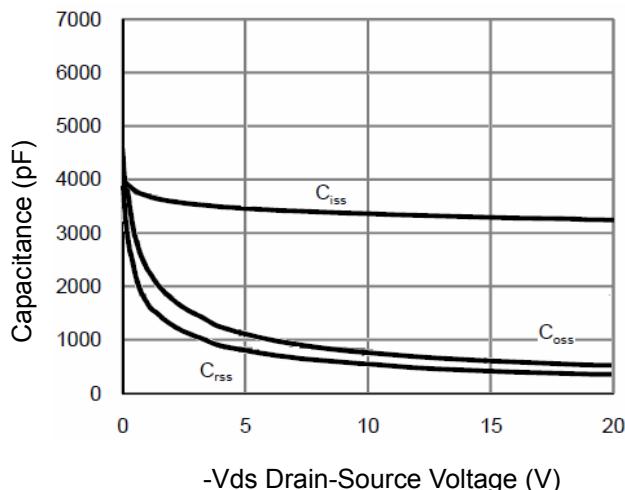


Figure 7 Capacitance vs Vds

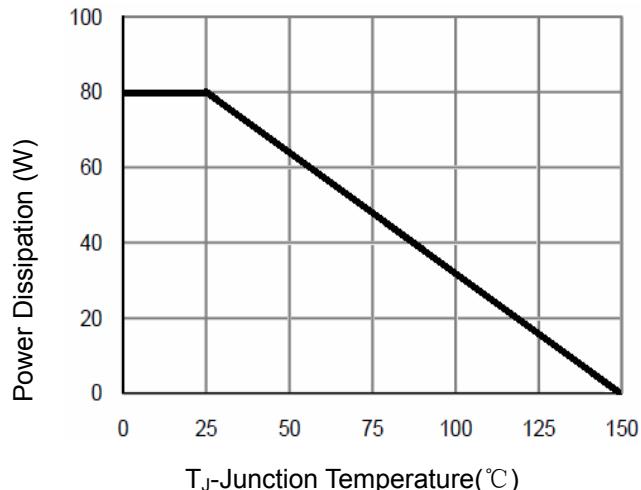


Figure 9 Power De-rating

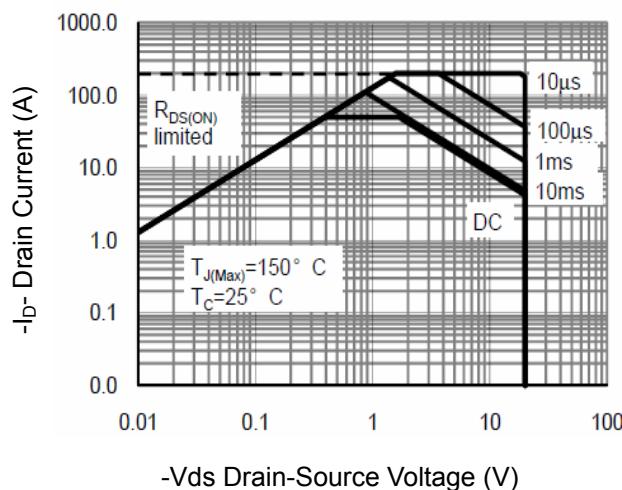


Figure 8 Safe Operation Area

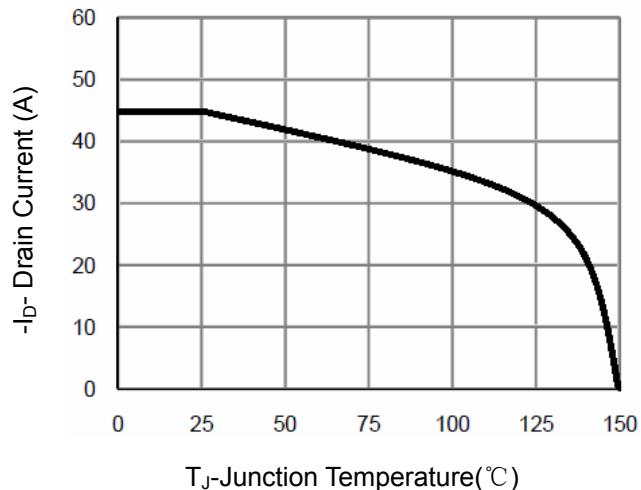


Figure 10 -Current De-rating

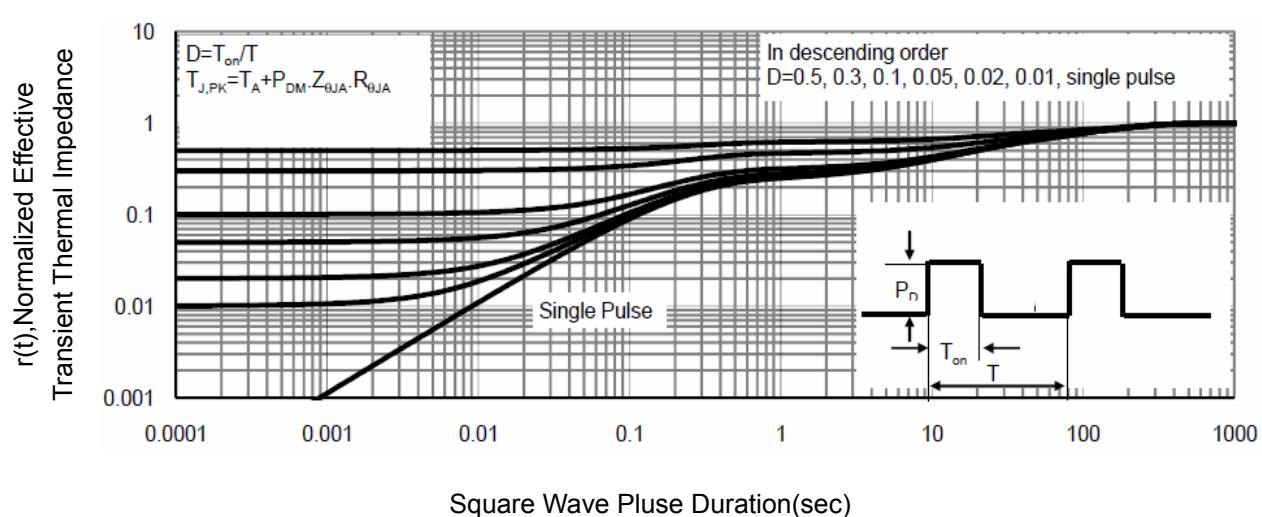


Figure 11 Normalized Maximum Transient Thermal Impedance

**DFN3.3X3.3 EP Package Information**

符号	单位: mm		
	MIN	MAX	TYP
A	0.75	0.85	0.8
B	0.25	0.35	0.3
C	0.18	0.22	0.2
D	3.2	3.3	3.25
E	3.2	3.3	3.25
F	2.2	2.5	2.35
G	1.8	2.0	1.9
H	0.3	0.4	0.35
I	0.15	0.25	0.2
J	0.4	0.5	0.45
K	0.6	0.7	0.65
L	1.38	1.58	1.48
M	1.8	2.1	1.95
N	0.15*45°		
O	0.4	0.5	0.45

